Design Document

**Concatenated Codes in**

**Amateur Radio Satellite Telemetry**

Submitted To:

Professor Dennis Silage

Senior Design Project I and II

Temple University

College of Engineering

1947 North 12th Street

Philadelphia, Pennsylvania 19122

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Prepared By:

B. Keith, B. Thibodeau, and C. Destin

Faculty Advisor(s): Dr. Dennis Silage

Programmable Communication Group

Temple University

College of Engineering

1947 North 12th Street

Philadelphia, Pennsylvania 19122

For further information, please contact Dr. Dennis Silage (email: silage@temple.edu).

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| **Team SD1-01** | **Programmable Communication Group** | **PCG** |
| **Team Members** | Brandon Keith, Brian Thibodeau, Cedric Destin | |
| **Advisor(s)** | Dennis Silage | |
| **Coordinator** | Thomas Sullivan | |
| **Department(s)** | Electrical and Computer Engineering | |
| **Project Title** | Concatenated Codes in Amateur Radio Satellite Telemetry | |
| **Abstract** | Research done by engineers in the Amateur Radio Satellite community has shown that the current method of transmission for Amateur Satellites, the Frequency Shift keying (FSK), contains several deficiencies and few benefits are gained despite the current technology. Over the years, the Amateur Radio community has relied on outdated communication method to transmit telemetry data and has settled for poor error rates due to the FSK modulation scheme. As a result, engineers such as Phil Karn have presented improvements on the current transmitter\ receiver systems in attempt of reducing the cost necessary to install a transceiver’s station, which is currently based on the need of a high (SNR = 25dB). A more efficient approach to transmit and receive has been suggested, for improving the current telemetry systems. The Binary Phase Shifted Keyed modulation scheme certainly has a more affordable bandwidth than the older FSK signal, in addition to BPSK, source coding techniques is an additional way of improving the current systems. In summary our project looks at both modulating schemes unto an FPGA and analyzes the FSK modem and BPSK modem with and without error correction over an Additive White Gaussian Noise channel. | |
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**Executive Summary**

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# Problem

## Overall Objectives

It has been shown that forward error correction dramatically improves bit error rate performance (BER) in amateur packet radio satellite telemetry links (Hsiao, et. al, 2000). Additionally, it has been shown that binary phase shift-keying (BPSK) modulation is more reliable and bandwidth-efficient than audio frequency shift keying (AFSK) modulation (Hsiao, et. al, 2000). Being that average amateur satellite telemetry benefits from neither of these facts, this senior design project aims to demonstrate the degree to which forward error correction and interleaving techniques with BPSK modulation can improve the reliability of the average amateur satellite telemetry link. Consequently, this senior design project advocates for improved robustness in amateur packet radio communication systems, specifically in those systems dealing with satellite telemetry.

Amateur packet radio satellite telemetry is often unidirectional (simplex) and does not benefit from automatic repeat request (ARQ) like in other bidirectional (duplex) amateur packet radio communications (Hsiao, et. al, 2000). In other words, if even one bit of an AX.25 telemetry packet is received in error, the entire packet is discarded and cannot be re-transmitted (Karn, 1994). This means that beacon signals from the amateur satellites must be transmitted with enough power to ensure that the embedded telemetry packet is received without error (de Milliano, et. al, 2010). BPSK modulation with forward error correction combined with interleaving can supersede AFSK, resulting in greatly improved network reliability and power-efficiency in amateur packet radio satellite telemetry. The enhanced network reliability could lower overall power consumption in amateur telemetry satellites (de Milliano, et. al, 2010), resulting in two benefits: 1) reduced cost of satellite construction, and 2) making amateur telemetry satellites more technologically and financially accessible to amateur satellite operators by reducing the size, cost, and complexity of ground station antennas (Karn, 2011).

Hence, the ultimate goal of this senior design project is to demonstrate the improved network reliability and power-efficiency that results from implementing forward error correction and interleaving with BPSK modulation in amateur packet radio telemetry satellites and ground stations.

## Historical and Economic Perspective

The standard digital modulation scheme used for amateur radio very-high frequency (VHF) and ultra-high frequency (UHF) operation is Bell 202 (Capitaine, et. al, 2010). Bell 202 provides AFSK modulation using 1200 Hz and 2200 Hz tones, with a resulting data rate of 1200 b/sec. It is typically used in the physical layer of the AX.25 data link layer protocol and this has been the case since the early 1980s (Karn, 1994). In 1984, when Bell 202 was a fairly new standard in the amateur radio community, Steve Goode, K9NG, performed an exhaustive bit error rate (BER) performance analysis of a standard Bell 202 modem (Goode, 1984). Goode found that at least 25 dB of FM receiver quieting (25 dBQ) was necessary for high communication reliability. In other words, 25 dBQ or greater was required to accurately receive 98% of incoming packets, which corresponded to a BER of 1.6e-5. Ralph Wallio, WORPK, figured out that with this BER, there is only a 1.603% chance of accurately receiving 117 consecutive 256-byte AX.25 packets (Wallio). Wallio concluded that “this is as Goode as it gets” and it is virtually impossible to get better results without error correction.

This poor reliability performance is not exclusive to amateur radio terrestrial communications. In 1995, it was demonstrated that error detection alone is not robust enough for amateur radio microsatellite communications (Hsiao, et. al, 2000). Particularly in simplex satellite communications, the harsh environmental conditions coupled with the microsatellite’s characteristically low transmitter power made for very unreliable telemetry data links (Hsiao, et. al, 2000). It has been demonstrated that forward error correction, specifically convolutional encoding and decoding, can generally correct up to 75 percent of errors (Hsiao, et. al, 2000). It was also demonstrated that 1200 b/sec BPSK provides much more reliable transmission quality than 1200 b/sec AFSK, irrespective to whether the VHF or UHF amateur bands are used. Moreover, it was demonstrated that BPSK occupies a considerably smaller frequency bandwidth than AFSK while possessing excellent anti-interference properties. And with a general tenfold BER performance increase for both 1200 b/sec AFSK and BPSK over 144 MHz VHF, implementing forward error correction for amateur satellite telemetry was clearly demonstrated to be better than not implementing forward error correction.

In 2003, the AAU-Cubesat was one of the first pico-satellites to be launched into space. Moreover, the miniaturized satellite harbored a communication subsystem that implemented both forward error correction and interleaving over 9600 b/sec Gaussian minimum shift-keying (GMSK) AX.25 (Alminde, et. al, 2002). The enhanced robustness and data rate was justified by the fact that it had to transmit approximately 1461 kilobytes (kB) of telemetry and picture data per day. This simply would not have been possible had the satellite not utilized error detection and correction. However, it operated at 437.9 MHz, meaning that it was particularly difficult for the average amateur radio operator with a 2-meter radio transceiver to receive its telemetry data. This would particularly bother Phil Karn, KA9Q, who is a strong proponent of making robust satellite telemetry links accessible to the average amateur radio operator (Karn, 2011). Karn asserts that robust telemetry links (using forward error correction) reduce the cost of satellite construction and simplify ground antennas, making amateur radio satellite telemetry much more technologically and financially accessible to amateur satellite operators (Karn, 2011).

As amateur satellite designers foresee the next generation of miniature satellites (de Milliano, et. al, 2010), and as the next generation of amateur satellites equipped with robust communication schemes continue to ascend into space, and as miniature satellites become increasingly more financially and technologically accessible to amateur satellite operators, it must be clearly demonstrated to the amateur radio community how these advancements trump the ubiquitous 1200 b/sec AFSK AX.25. Hence, to reiterate, this senior design project hopes to clearly demonstrate the performance advantages that yield from using forward error correction and interleaving schemes with BPSK modulation in amateur satellite telemetry.

## Candidate Solutions

Typical functions of a modem include forward error correction, source encoding, modulation, demodulation and source decoding. In the last century, many solutions have been proposed that trade performance in terms of bandwidth, transmission power and complexity. In this section we consider two common types of forward error correction - block codes and convolutional codes, two line codes – Non-Return to Zero (NRZ) and Manchester code, and finally coherent and non-coherent demodulation techniques used for BPSK and FSK. This includes solutions for carrier recovery and timing recovery.

### Forward Error Correction: Block and Convolutional Codes

Forward error correction (FEC) is a form of robust channel coding. It is used to correct errors that are injected into a digital communication link across a noisy propagation medium. FEC codes fall into two general categories: block codes and convolutional codes. It is important to note that at the time of writing this document, the Xilinx CORE Generator in Project Navigator ISE 14.6 only consists of one block coder/decoder pair and one convolutional coder/decoder pair. The block coding pair consists of a Reed-Solomon coder and decoder. The convolutional coding pair consists of a convolutional encoder and a Viterbi decoder. Hence, the FEC engine will be limited to using these channel code pairs.

In Section 1.3.5, we discussed that the satellite communication link is vulnerable to random errors and burst errors. Block codes are better suited for correcting burst errors while convolutional codes are better suited for correcting random errors (Viswanathan, 2013). A combination of block codes and convolutional codes, namely a two-level coding system, are used in many systems to provide robustness against both kinds of errors (see Figure 9). This two-level coding system consists of a coding chain and a decoding chain. The coding chain resides in the transmitter and consists of a Reed-Solomon encoder, followed by an interleaver, then a convolutional encoder. The decoding chain resides in the receiver and undoes what the coding chain did. Namely, the decoding chain consists of a Viterbi (convolutional) decoder, followed by a de-interleaver, then a Reed-Solomon decoder.



Figure 9. Top-level diagram for the FEC engine (System C) consisting of a block code pair, an interleaving pair, and a convolutional code pair.

### Line Coding: Non Return Zero and Manchester

There are three criteria used for evaluating the performance of line codes, interference and noise immunity, bandwidth, and synchronization capabilities. These criteria are used for determining the appropriate line code that should be used in our modems. NRZ is the most common line code as it appears naturally in digital logic. A ‘1’ is represented by a positive voltage while a ‘0’ is represented by zero voltage. Conversely, Manchester line code represents a ‘1’ by a transition from zero volts to a positive voltage during the second half of the bit period while a ‘0’ is encoded as a transition from a positive voltage to zero volts during the first half of the bit period. Compared to NRZ, this means that Manchester code has two level transitions during one bit period while NRZ has only one. This presents a tradeoff between NRZ and Manchester in terms of synchronization and bandwidth. The two level transitions during each bit period means that the receiver can more easily extract a clock used for synchronization between the transmitter and receiver. The tradeoff is increased bandwidth due to the more frequent transitions, but how do these line codes perform in a noisy environment? The simple answer is that they perform the same. It can be shown that the energy in NRZ and Manchester is where is the bit period. It can also be shown that each line code has a theoretical probability of bit error to be:

Since they both share the same theoretical probability of bit error and contain the same energy, they both perform equally likely in a noisy environment. Thus the decision for choosing NRZ or Manchester resides in what is more important, bandwidth or synchronization? Considering our modem requires only a 1200 b/sec data rate, it was decided that synchronization was more important than bandwidth. Thus the line coding that will be used in both the FSK and BPSK modem will be Manchester coding.

### BPSK Carrier Recovery

The demodulator is responsible for providing either coherent or non-coherent demodulation. Coherent demodulators require phase synchronization between the received signal and the locally generated oscillator. Conversely, Non-coherent demodulation does not require synchronization and makes no attempt to estimate the phase of the received signal. The advantage of non-coherent modulation is that it does not require additional hardware like phase-locked loops which are used to lock onto the incoming carrier phase (Feigin, 2002). However, the LEO-AMSAT’s we are interested in communicating with use BPSK for downlink and thus requires the design of a coherent demodulator.

The successful extraction of information from a received signal in a coherent demodulator requires both carrier and timing synchronization. Figure 1 illustrates the architecture of a typical coherent demodulator.



Figure 1. Received waveform takes two paths. First path extracts carrier for coherent demodulation and the second path recovers timing information. This architecture is based on the optimum binary receiver

The received signal from the transceiver is first processed by a band pass filter to remove as much noise as possible and then sent to the carrier recovery circuit. Recovering the carrier is done in one of two ways, the squaring loop or the Costas loop. Each method utilizes phase-lock concepts and has its own advantages and disadvantages in terms of complexity and performance.

**Carrier Recovery using Squaring Loop**

The squaring loop is a popular choice for coherent demodulation of BPSK waveforms. It’s mathematically easy to analyze and its hardware implementation is not as complex as the Costas loop. As the name implies, the received signal is squared to remove any phase offsets and then processed by a bandpass filter to remove as much noise as possible. After the band pass filter, the signal is fed to a phase-lock loop (PLL) for phase and frequency tracking. Once the output of the voltage controlled oscillator (VCO) is locked in phase and frequency with the received signal, its frequency is divided by two. The resulting carrier is fed back to the mixer where it is mixed with the received waveform and the timing can be recovered (Nguyen & Shwedyk, 2009). The operation of the squaring is shown in Figure 2.



Figure 2. Squaring loop used for carrier recovery in the coherent demodulator. The Phase-Lock Loop utilizes feedback to track and lock onto in the received waveforms suppressed carrier

**Carrier Recovery using Costas Loop**

The second method for carrier recovery is the Costas Loop. Unlike the squaring loop whose only purpose is suppressed carrier reconstruction, the Costas loop is capable of synchronous data detection in addition to suppressed carrier reconstruction (Feigin, 2002). One of its disadvantages is its mathematical complexity compared to the squaring loop, but in terms of hardware components needed for complete coherent demodulation, they both require approximately the same amount.



Figure 3. Costas loop used for suppressed carrier reconstruction as well as synchronous data detection.

Coherent modulation utilizing the Costas loop would require one band-pass filter, three low-pass filters, three multipliers and a VCO. Likewise, the squaring loop would also require one band-pass filter, three multipliers (including the squarer) and a VCO. Instead of three low-pass filters needed by the Costas, the squaring loop only requires two. Note also that the squaring loop requires a flip-flop for frequency division, but with today’s FPGA’s, a single flip-flop is negligible. An alternative to this is a phase lock loop configured as a fractional-N-frequency synthesizer (Crawford, 2008).

Following analytical and experimental analysis of both the Costas loop and squaring loop in Simulink, it was decided that we implement the squaring loop for BPSK carrier recovery. The mathematical complexity of the Costas proved difficult to derive an accurate transfer function that described the loop’s behavior. Conversely, the squaring loop uses a phase lock loop in which literature was rich and plentiful. We were able to derive a transfer function that accurately modeled the loops behavior. This is important because it allows us to confidently compensate for phase and frequency offsets in addition to tuning transient performance that minimize bit error.

### Coherent and Non-Coherent BFSK Modulation (Cedric)

The BFSK modem abides by the Bell 202 standard which uses frequencies of 1200 Hz for Mark (*b0*) and 2200 Hz for Space (*b1*). Following this protocol, the phase of the signal can be implemented either coherently or non-coherently. A coherent modulation (continuous phase modulation) implies that the phases of the two tones representing the data are always the same, which inherently prevents discontinuous jumps between a Mark and Space. Conversely, non-coherent FSK modulates the two signal waveforms without any effort to match the two signals’ phase, hence the modulated signal may experience discontinuous jumps in phase.

Coherent FSK modulators tend to consist of several complicated components, and therefore are not commonly used to avoid unnecessary loss of power although they yield a better BER performance (Rao et. al, 1990). On the other hand Non-coherent FSK modulation is simpler to implement and is commonly used in several modulation despite its BER performance compared to the coherent modulation. However, with the technological development, coherent modulation can surely be implemented with as much efficiency as the non-coherent modulation.

**Non-coherent modulation**

As previously mentioned, coherent modulation requires continuous phase of the modulated signal, which can involve complicated hardware or algorithms. As a result, it is common to ignore the phase of the signals and directly modulate the two signals. This implies that the phase modulated signal will be subject of random variations. The non-coherent modulator can be implemented using the two sinusoidal wave generators or two sine functions and a multiplexer controlled by the input data *m(t)*. Switching between the frequencies will generate a BFSK waveform with a bit period equal to the periodicity of the switches.



Figure 4. BFSK modulator used in non-coherent modulators. The data *m(t)* controls the output of the multiplexer at data’s baud rate.

**VCO Coherent modulation**

Non-coherent waveforms originate from the fact that two totally different sources are used to modulate the data, therefore the phase resulting from the modulator varies as signal is altered through the two tones. Using a single source to modulate will maintain a continuous phase as expected. Voltage Controlled Oscillators are commonly used to provide a continuous phase, and generate a sinusoidal wave based on the input control signal.



Figure 5. Coherent modulator for BFSK. The data *m(t)* controls the output of the VCO through Eq. 3

### Coherent and Non-Coherent BFSK Demodulation (Cedric)

The Bell 202 Protocol is quite complex due to the frequency deviation and the ratio between the data rate and carrier frequency. The Bell 202 modem uses frequencies with a small frequency deviation from the carrier frequency to represent it binary data and where the tones selected are 1200 Hz and 2200 Hz. The frequencies selected to represented two symbols result in a signal space that is difficult to optimize since the frequencies are not orthogonal as the minimum frequency separation is denoted in equations (3) and (4) below (Nguyen, et. al, 2009).

**Coherent demodulation**

Similar to the modulator, the demodulator can be categorized into a coherent modulator and a non-coherent demodulator. In the coherent demodulator, the phase of the modulated signal is either known or is extracted prior to demodulation. Several methods are used to extract the phase of the modulated waveform, such as the phase-lock loop or more complicated systems as illustrated in Figure 6.



Figure 6. Coherent modulator for BFSK. The data *m(t)* controls the output of the VCO through Eq. 3

The coherent demodulator in Figure 6 uses two parallel branches for matching the Space and Mark onto the two orthonormal basis functionsand. Finally, using the appropriate threshold and decisions, the bits can be recovered using Maximum Likelihood. The correlation receivers or matched filters and are designed to be orthonormal to each other, and at a frequency corresponding to the Mark and Space signals. The process of using matching filter results in an optimum demodulator in terms of BER and can even be reduced to a single correlation receiver according to the relationship shown in equation (5).

The use of a phase lock loop is also a valid method for demodulating FSK. The PLL has been integrated in several radio for demodulating FM and can also serve to demodulate FSK signals. In the case of non-coherent signals, the PLL acts as an estimator of the frequencies and phases (Rao et. al, 1990) by rapidly matching the output of the VCO, the PLL is used to appropriately estimate the correlation between the signal and the output of the VCO. This is illustrated by the block diagram in Figure 8.

****

Figure 8. Coherent demodulator for BFSK using PLL.

**Non-Coherent demodulation**

In the case of a signal with discontinuous phase non-coherent demodulation is regarded as the ideal demodulator in FSK modulation. The advantage of non-coherent demodulator come from their ability to ignore the phase change contained in the signal. Matched filters are still utilized however, an envelope detector is present in each branch after each tone’s matched filters.

The matched filters are configured with the same objective as the coherent receiver, and the use of the envelope detector removes the phase changes. The performance of the non-coherent demodulator results in performances that closely approach the performance of the optimum coherent receiver. (Linsey et. al, 1977)(Rao et. al, 1990)

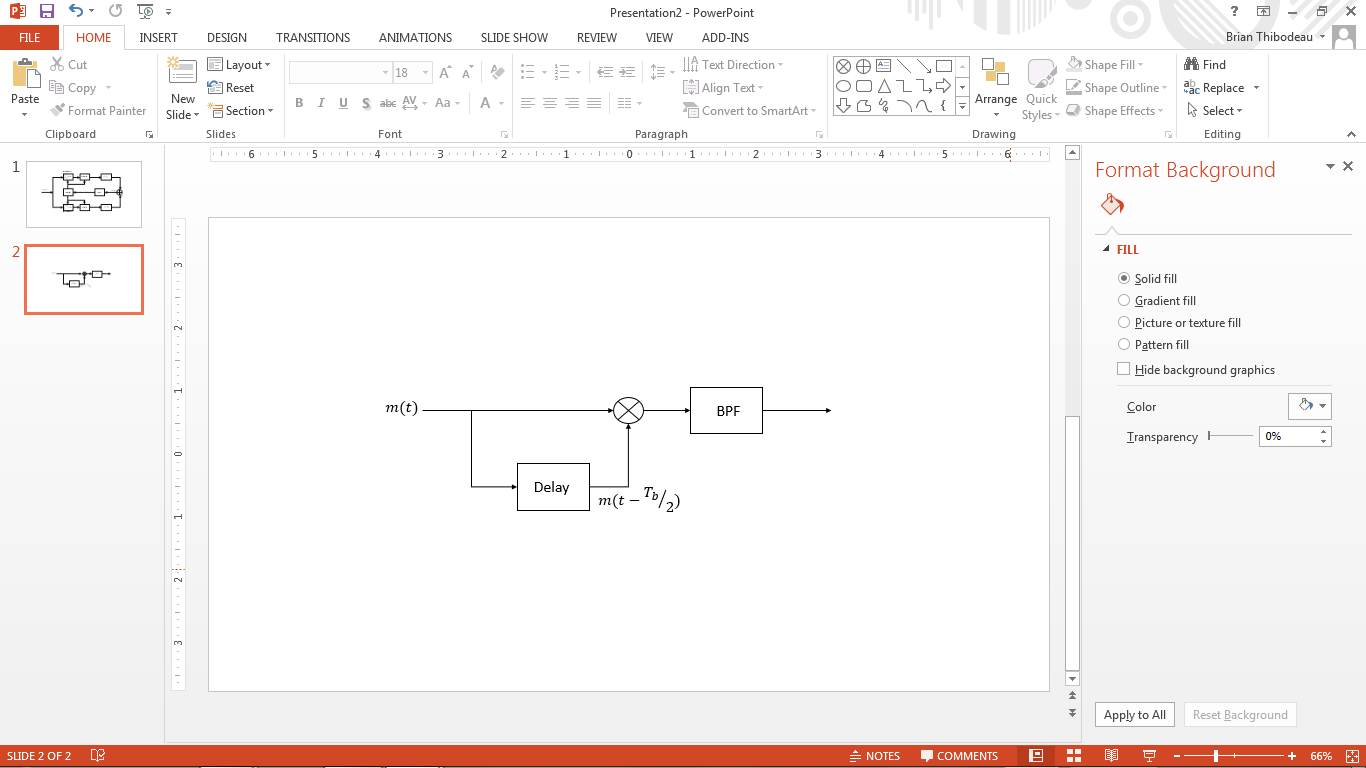


Figure 7. Non-coherent demodulator for BFSK, where the Mark and Space filters are centered at 2200Hz and 1200Hz respectively.

### BPSK and BFSK Timing Recovery

Timing recovery is the process of extracting a clock from the received signal so that the correct symbol determination can be made. The reason for this can be understood by recognizing that the local clock at the receiver is not synchronized with the transmitter clock and does not know when to sample the received data in order to make the correct symbol determination. In this section we consider two non-data aided architectures used for timing recovery. The first is an open loop architecture which is shown in figure 1a and the second is a closed loop architecture shown in 1b. The closed loop timing recovery circuit is known as the early late-gate.

In both methods it is assume that the received signal is baseband and contains no spectral component. Thus the problem is similar to carrier phase recovery in BPSK. In the open loop method, a spectral component is created by delaying the received signal by one half a bit time and then multiplying it with the original received signal. The result of the multiplication produces a spectral component at a rate of Hz. Then



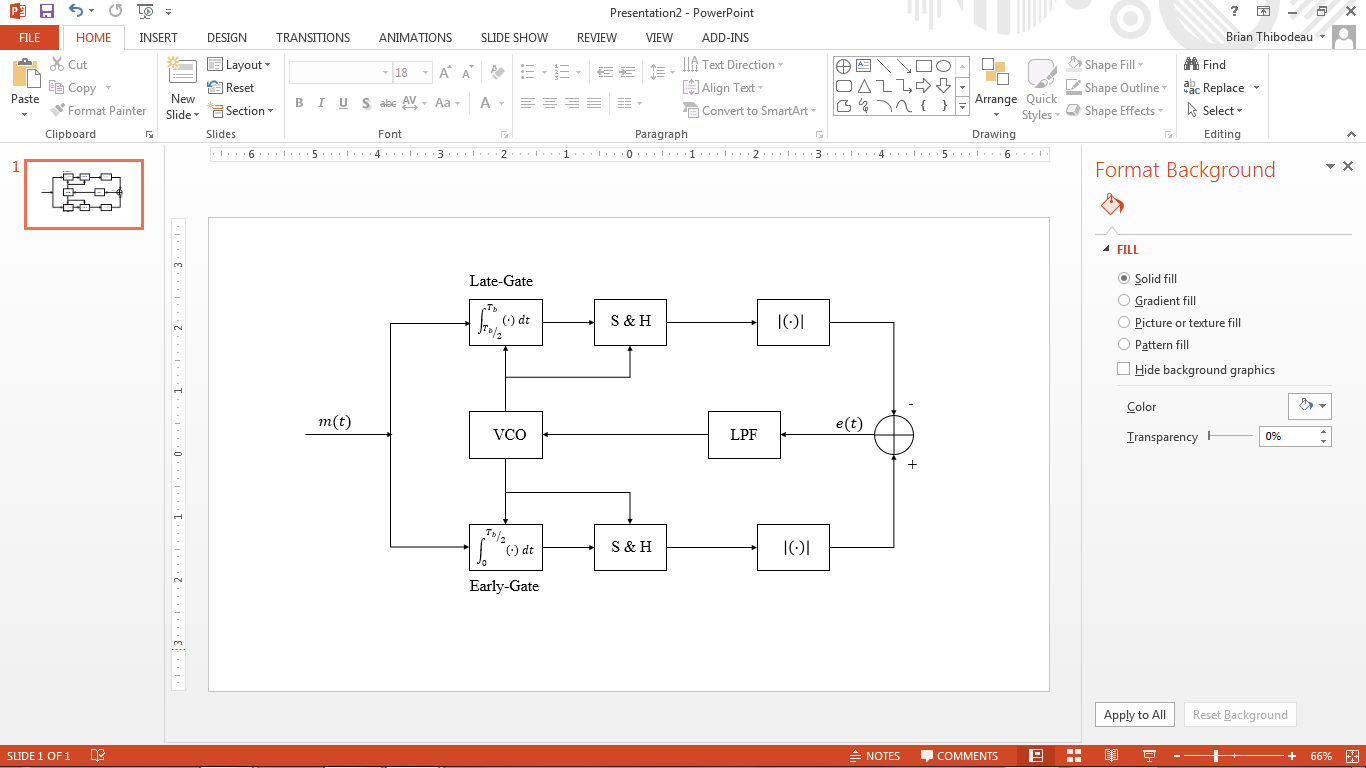
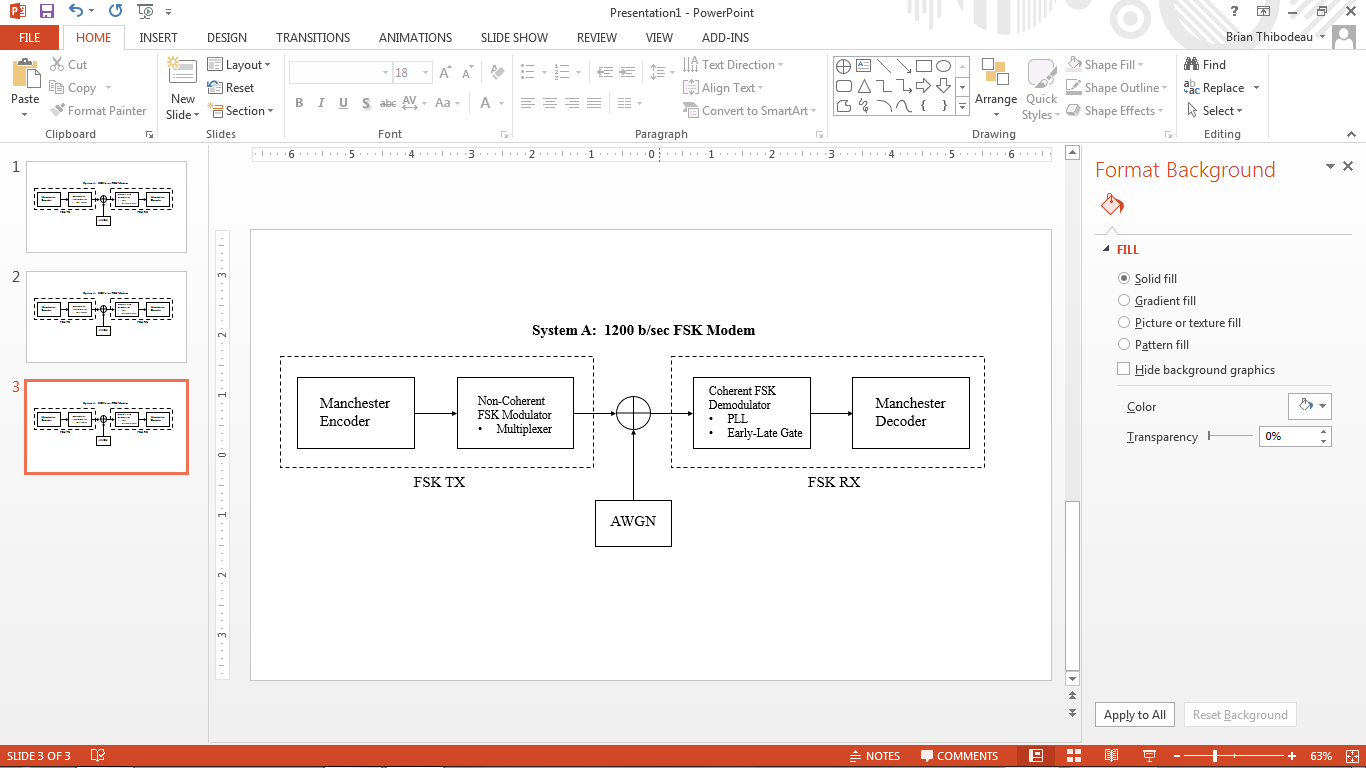


Figure 1

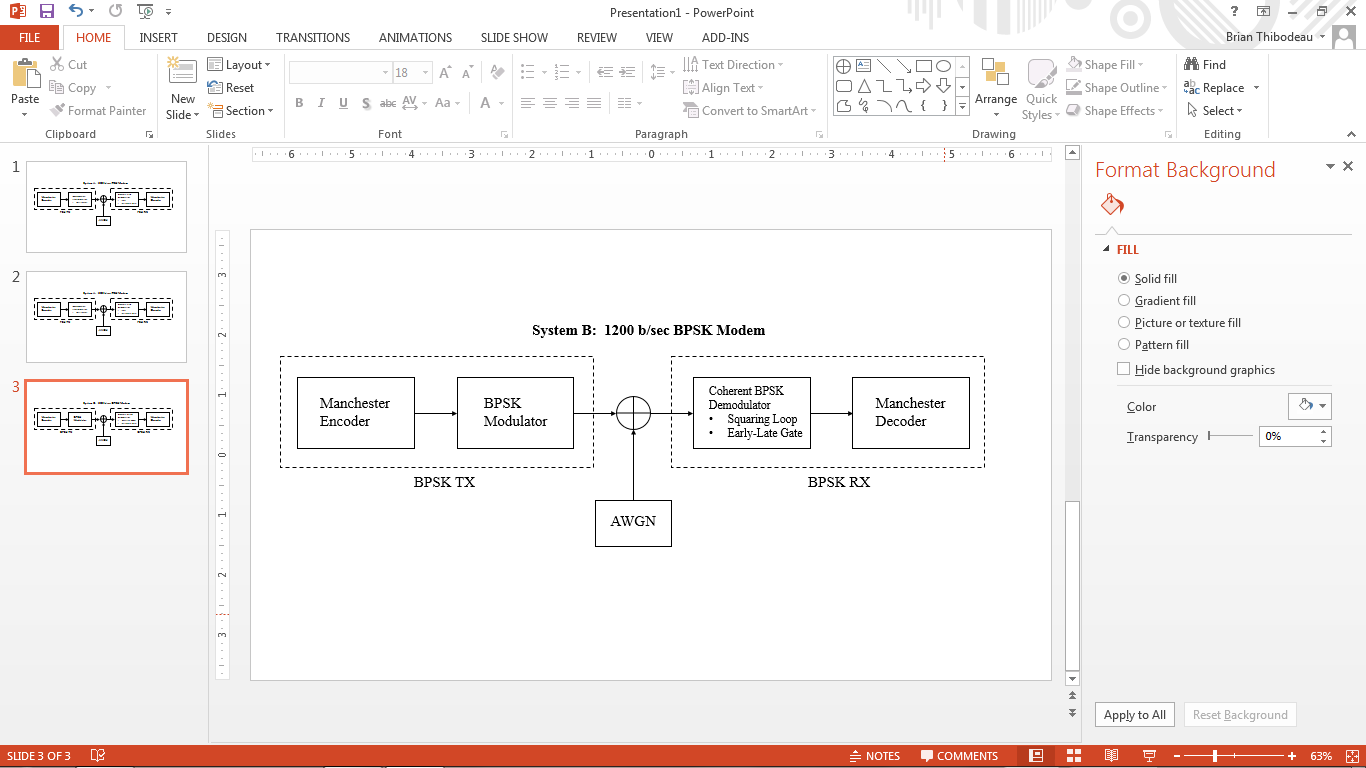
a simple band pass filter can be designed to isolate the desired spectral component. Although simple to implement, the problem with the open loop method is that there is an average non-zero tracking error that reduces system performance (Nguyen & Shwedyk, 2009). This problem is alleviated by using a closed loop feedback architecture shown in figure 1b. The principle idea behind the early-late synchronizer is to sample the received signal at different times and compare the two to generate an error. The error signal drives a VCO which advances or retards the clock until the error is zero (Judd, 1996). When the error is zero, the output clock from the VCO is used to sample the received signal at the optimal time needed for correct symbol determination. Since the Early-Late gate synchronizer results in zero error, this method was chosen for timing recovery in our modems. A detailed analysis of its operation is discussed in the Approach.

## Proposed Solution Concept

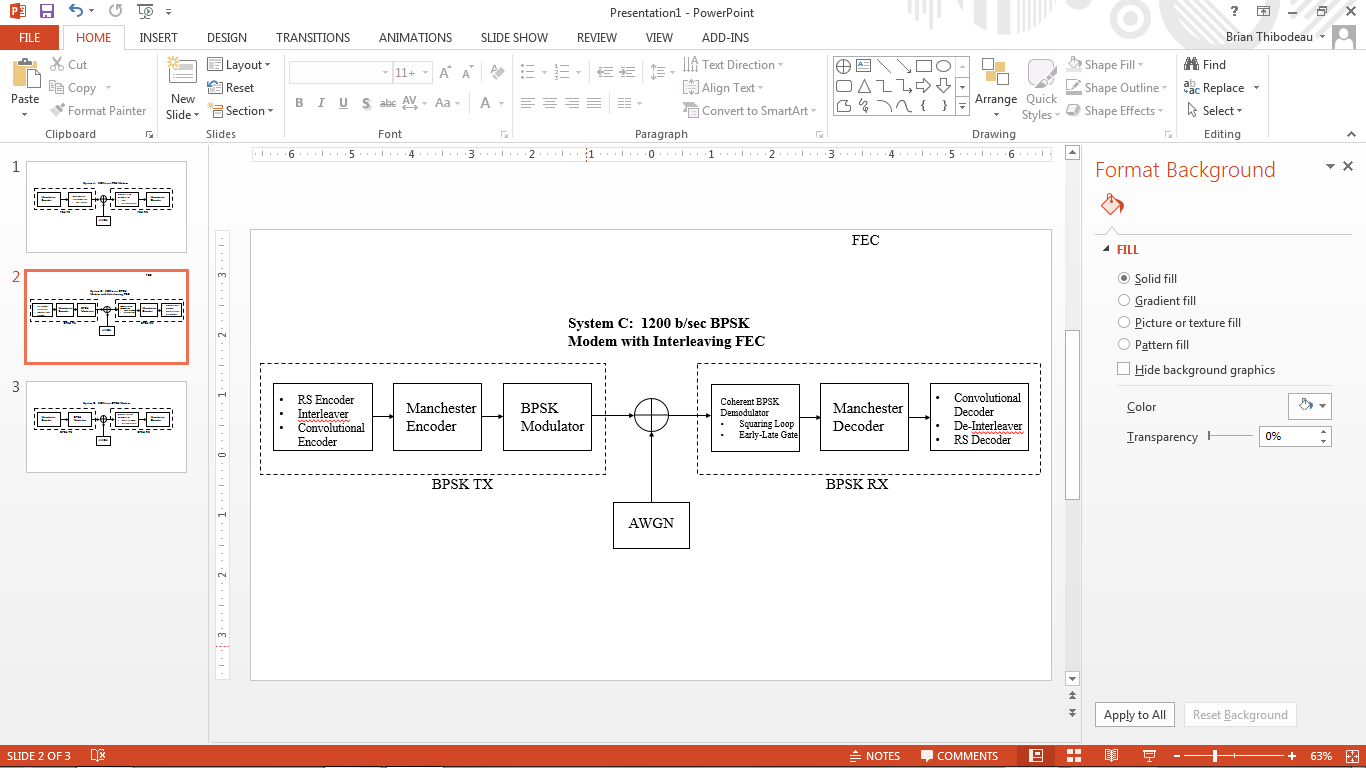
This senior design project will determine the telemetry packet error rate (PER) performance and the coding gain due to implementing forward error correction in amateur radio satellite telemetry. These two parameters, respectively, will allow us to compare the reliability and power-efficiency between using and not using FEC in amateur radio satellite telemetry. This implies that we will be comparing several digital communication systems. In this senior design project, three digital communication systems will be developed for modeling amateur radio satellite telemetry. The first system (System A) will replicate most amateur radio satellite telemetry links that exist today – 1200 b/sec Bell 202 modulation without FEC. This FSK modem will perform Manchester encoding and noncoherent modulation. Demodulation in the FSK modem will be accomplished coherently through use of a PLL while timing recovery is accomplished by the early-late gate synchronizer.



The second system (System B) will exploit the fact that BPSK modulation is better than AFSK in amateur VHF and UHF operations (Hsiao, et. al, 2000) – 1200 b/sec BPSK *without* FEC. This system will also perform Manchester encoding and decoding in addition to suppressed carrier reconstruction using a squaring for suppressed carrier reconstruction. Like the FSK demodulator, timing recovery is also accomplished through the early-late gate synchronizer.



The third system (System C) will be a robust version of system B – 1200 b/sec BPSK *with* FEC. FEC correction will be accomplished by use of both block and convolutional coding. The addition of interleaving between the block and convolutional encoding will further improve the reliability of the BPSK modem.



## Major Design and Implementation Challenges

The three systems discussed in Section 1.3 (Candidate Solution) will each have their specific requirement to complete the intended analysis between each system. The general implementation of each system on FPGA is intended to be simulated under common *a common signal distortion* where the Additive White Gaussian Noise transmitting channel will be used for all three systems on purpose of evaluating their respective performances when used in satellite communication. Hence, an Intellectual Property from Xilinx will be ideal to fully complete the analysis of each systems.

In terms of System 1 (FSK modem,) a coherent demodulator which follows that of the common Bell 202 modems is required to analyze the past designs to an innovative communication design. The demodulator is expected to resemble the present methods used in Amateur Radio Satellite operators, using discrete components implemented in FPGA. The coherent PLL demodulator is then designed using controls theory to demodulate signals with similar SNR as previous modems under the standard Bell 202 protocol.

The BPSK components of System 2 and 3 is expected to demodulate the incoming BPSK signal using the Squaring Loop designed using controls theory. The squaring loop is expected to regenerate the carrier frequency under severe SNR conditions, hence the senior design project faces the challenges of designing a robust demodulator using the squaring loop for BPSK demodulation. The PLL is also expected to endure frequency changes that may be as large as double the carrier frequency used therefore the ramp response of the PLL’s transfer function also be minimized, as well as the acquisition time to minimize the loss data.

The error correction section of System 3 is intended to feature correction for burst of errors and random errors which may occur during transmission of data. Hence, a block encoder is expected to have an optimized code rate to enable the correction of numerous burst of errors occurring. Because of the complicated algebra involved, complexity in the design of the block encoder must be avoided, and such challenge poses an immediate constraint on the design project when designing the error correction. Similarly, the design of the block interleaver aim towards an optimized interleaver’s depth, (*d*.) Both of those parameters must also be considered at the receiver where decoding and de-interleaving occur to remove the coding done at the source. A very large depth will result in a slower computation at the receiver, hence, the depth must be optimized to optimize both the computation time at the receiver and the robustness of the system with respect to burst of noise and random noise.

The Systems 1, 2, and 3 all need to include data recovery ability to fully recover the baseband signals. In all systems, data recovery needs to correlate, sample depending on the recovered clock of the transmitter. Such synchronization process is done using the Early-Late Synchronization technic on all three receivers of the Systems.

## Implications of Project Success (Brandon)

It was hinted in Section 1.1 (Overall Objective) and Section 1.2 (Historical Perspective) that this senior design team has identified a problem within the amateur radio community. According to amateur radio operator Jeff Davis, KE9V, amateur radio has somewhat of a *lost future* (Davis, 2010). In the earlier half of the 20th century, amateur radio operators led the forefront of “discovery and experimentation” in the industries of electronics and communications. This was the case because many amateur radio operators were in fact professional electronics technicians and electronics engineers that designed and implemented the next wave of commercial and military communications. Oftentimes, the budding amateur radio operator, a *neophyte* if you will, would go on to become the next electronics repairman or electronics engineer. However, Davis highlights the fact that at some point in the past, the amateur radio community reached somewhat of a crossroads. Up to that point in time, the amateur radio community had pioneered Frequency Modulation (FM) communications over ultra-high frequency (UHF) and very-high frequency (VHF) operations, stationed repeaters throughout the land for long-distance over-air communications, and launched amateur radio satellites into the heavens which led to improved methods for space communications in addition to low-cost spacecraft manufacturing and launch. Davis highlights the fact that although the non-amateur world would go on to produce cellular technology, drastically improved over-air communications, and intelligent military digital communications, the amateur radio community as a whole decided to dwell in the past as the future marched ahead without it.

This senior design team identified one amateur radio operator and notable electrical engineer, Phil Karn, KA9Q, in his efforts to secure the future of amateur radio. Like Jeff Davis, Phil Karn is also aware of amateur radio’s *lost future*. In a modem design article (Karn, 2011), Karn hints that making amateur radio communications more accessible to prospective amateur radio operators is one solution for securing the future of amateur radio. Specifically, in the design article, Karn identifies the fact that amateur radio satellite communications is mostly inaccessible to amateur radio operators because the equipment involved is too expensive and esoteric. Karn’s philosophy is that by making amateur radio satellite communication accessible to all amateur radio operators, school demonstrations will be more commonplace and consequently more kids will want to become amateur radio operators. It is implied that if more kids become amateur radio operators, or *hams*, amateur radio in general cannot have a *lost future*.

Hence, according to Phil Karn, one solution to securing the future of amateur radio is to make amateur radio satellite communications more accessible to kids. In order to make amateur radio satellite communications more accessible to kids, the amateur radio equipment involved in said communications must be less expensive and esoteric. By expensive and esoteric, Karn is referring to software-defined radio systems and bulky antennas. This kind of equipment is regarded as being too inaccessible for the typical school demonstration of amateur radio satellite communications. Instead, Karn emphasizes the fact that a standard 2-meter single sideband (SSB) transceiver and an inexpensive antenna system should be all that is required at these school demonstrations. Satellite communications in general requires for relatively high-powered transmission of signals to overcome the high fading (energy loss) that results from an electromagnetic wave propagating through space (Sklar, 2001). In fact, free space attenuates an electromagnetic wave more than any other form of power attenuation along a satellite communication link. Hence, it is often the case that transmitted signals between amateur packet radio satellites and ground stations either deal with high transmission power to acquire a digital communication link with high data reliability or lower transmission power and low data reliability and link efficiency. It is understood that if you increase the reliability of a communication link, you can consequently get away with communicating at a lower signal-to-noise (SNR) ratio (Sklar, 2001). This results in lower transmitted power between an amateur radio satellite and ground station. Being that the power amplifier of the transmitter utilizes the most power of an amateur radio satellite, the lower power requirement could result in cutting the cost of satellite construction and simplify the ground antennas (Karn, 2011). Consequently, amateur radio satellite communications would become more *accessible* to prospective amateur satellite operators.

In a similar fashion as Phil Karn, KA9Q, and others (Hsiao, 2000), this senior design project aims to demonstrate that there are much more power-efficient digital communication schemes than are currently employed in most amateur radio satellites today. The intention of this senior design project is to provide concrete evidence that BPSK modulation and concatenated error-correcting codes can make amateur radio satellite communications more power-efficient and hence, more *accessible* to prospective amateur satellite operators. Perhaps a simple BER performance analysis of popular and prospective communication schemes, like showcased in this senior design project, would further persuade an amateur satellite designer to employ more power-efficient communication schemes in the increasing fleet of miniaturized amateur radio satellites.

# DESIGN REQUIREMENTS

As discussed in the section 2.4, our analysis will require the design and implementation of three systems in FPGA in order to demonstrate that interleaving FEC in BPSK provides better performance than the BELL 202 and BPSK without interleaving FEC. The functional requirements of each system are summarized in Table 1. of section 3.1 followed by a summary of each. Non-functional requirements are listed in Table 2 of section 3.2.

## Functional Design Constraints (Brian)

|  |  |
| --- | --- |
| **Name** | **Description** |
| Bit Rate | Each modem is required to modulate 1200 b/sec data with the locally generated oscillator in order to communicate with the 1200 b/sec PACSATS. |
| Line Coding | Manchester Encoding is resilient to small changes in Frequency due to Doppler shift and provides easier clock extraction during demodulation. |
| Modulation/ Demodulation | FSK modulation is performed non-coherently while demodulation in FSK and BPSK is done coherently. |
| Operating Frequencies | Per Bell 202 standards, FSK modulation uses 1200 and 2200 Hz tones for Mark and Space. The BPSK modems will modulate that data using 2400 Hz carrier |
| Signal to Noise (SNR) | BPSK modem *without* FEC should provide a 6 dB performance increase over FSK modem. BPSK modem *with* FEC is expected to provide another 6 dB increase over BPSK modem *without* FEC |

Table 1. Functional design constraints for the all three systems.

Since 1200 b/sec Manchester encoded data streams are typically used for telemetry in Amateur Radio satellites, we require that both our FSK and BPSK modems follow these same requirements. We want to keep the attributes and characteristics of the FSK and BPSK modems as similar as possible in to demonstrate the BPSK *with* FEC reduces the required transmission power while reducing BER. In accordance with the Bell 202 standard for AFSK, the FSK modem will modulate the 1200 b/sec Manchester data stream using audio tones of 1200 Hz and 2200 Hz for mark and space respectively. However BPSK signals are typically modulated by a carrier that is an integer multiple of the bit period (Nguyen & Shwedyk, 2009). Thus a 2400 Hz carrier is chosen for BPSK modulation.

As the objective of this project is to demonstrate the performance increase of BPSK *with* FEC we require that the addition of FEC provide at least a 6 dB reduction in SNR compared to the BPSK modem *without* FEC. Since BPSK *without* FEC has already been shown a 6 dB performance increase over AFSK, we expect that we interleaving FEC can add another 6 dB performance increase (Magiliacane, 1999).

## Non-Functional Design Constraints (Brandon)

These non-functional design constraints are based off of the Papilio Pro LX9 FPGA development board and the Xilinx Spartan 6 XC6SLX9 FPGA.

|  |  |  |
| --- | --- | --- |
| **Type** | **Name** | **Description** |
| Economic | Cost | Board: $85 - $100 |
| Environmental | Temperature | FPGA: 0°C to +85°C |
| Environmental | Power Consumption | Board: maximum 600 mA @ 3 V |
| Manufacturability | Dimensions | Board: 3 in. wide x 4 in. length x 0.5 in. height |
| Manufacturability | Weight | Board: 32 grams |

Table 5. Non-functional design constraints for test board.

# APPROACH

## Software Simulation Using Matlab/Simulink

Simulink provides a graphical design approach for rapid prototyping and simulation of the various subsystems required by each of the modems. Thus the FSK and BPSK modems were first designed in Simulink which enables us to gain a high level operational understanding of each modem. In addition, Simulink provides the tools and blocks necessary to evaluate the performance of our system under a variety of conditions. Of particular importance was the evaluation of system performance due the effects of AWGN and phase and frequency shifts. These are conditions that all modems are expected to able to handle.

The remainder of the section is organized as follows, section 4.1.1 will consider the Simulink design of the Manchester encoder and decoder that is used in both the FSK and BPSK modems. In section 4.1.2, the FSK and BPSK modems design is discussed. Then in 4.1.3, coherent demodulation of both FSK and BPSK is discussed by examining the phase lock loop. Each modem has slightly different requirements for the PLL and thus its application will be examined for FSK and BPSK. Closely related to PLL is the early-late gate synchronizer which is used for timing recovery of both modems. Its Simulink designed will also be discussed in section 4.1.3. Lastly, 4.1.4 will conclude the Software simulation section by examining interleaving forward error correction and how it can be used to reduce the BER of the BPSK modem.

### Manchester Encoder/Decoder

The binary digits from the computer (TNC) are abstract values and need to be converted to tangible waveforms. In wireless communication, Manchester code has established itself as a standard signaling technic among the several others. Signal techniques are chosen depending on several criteria among those criteria, synchronization is an indispensable component of the receiver. Being that Manchester code contains such criteria improves the synchronization process being, hence it may be referred as a self-clocking signaling technic.

Manchester code is also not a complicated signal scheme to implement and needs few components to obtain a self-clocking behavior. Hence, Manchester code has gained a great amount of popularity among communication engineers, being implemented in various Amateur Radio communication and also has been a standard protocol for Ethernet. The IEEE standard protocol maps the binary values and into negative and positive edges of a square waveform only during the falling edge of the clock. Therefore, transitions at the positive edges of the clock contain no information, Figure # illustrates the protocol from the IEEE 802.3 protocol where and.

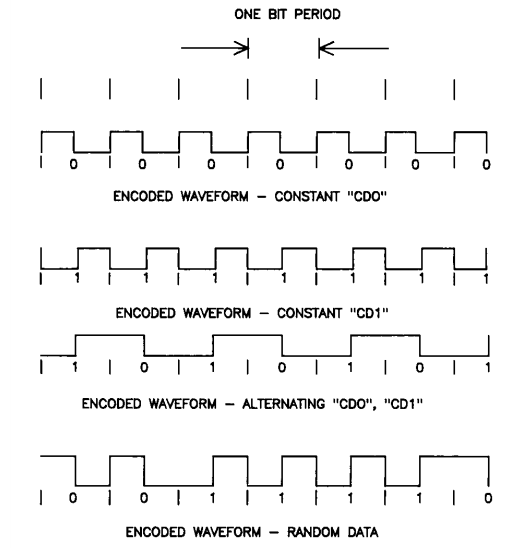


Figure #: Manchester code based on the IEEE 80.3 standard for Ethernet (IEEE, 2012)

Implementing the Manchester code can be done either using switches or the XOR logical operator () as depicted in the Figure # + 1. Therefore Manchester code is implemented in Matlab Simulink by XORing a stream of random data with the transmitter's clock which for the BPSK modem and BFSK modem has a bit rate of 1200 b/sec. Further modification can also be done by altering the magnitude values of the signal waveform, either

Where the latter is referred as the Manchester code- Leveled.

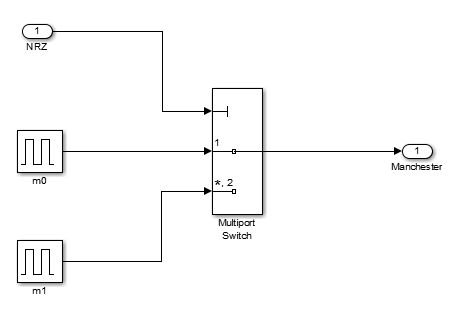
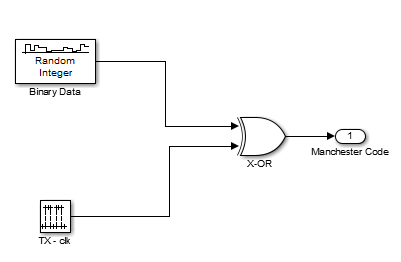


Figure # + 1: Manchester encoder using an XOR gate (left) Multiplexer (right)

At the receiver, the data must also be decoded to extract the information from the coded signal. The decoder is done using the Manchester code basis function denoted as. Decoding the Manchester code yields very accurate results due its efficient geometrical properties. The correlation coefficient between the two signaling waveforms equals to, hence the Manchester encoding provides a maximum distance between the waveforms as illustrated by (Nguyen et al). In the modems, the decoding is also done following the same approach, where the product between the encoded waveform and the extracted clock is used to recover the binary digits.

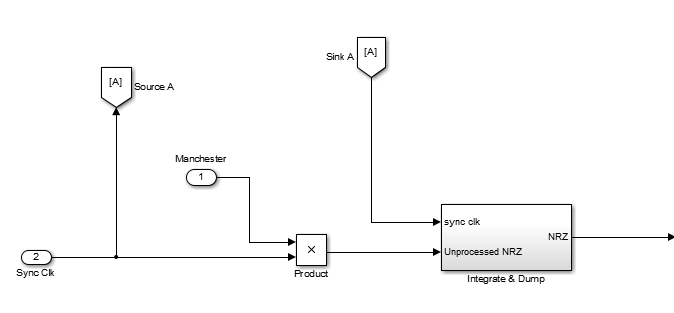


Figure # + 2: The decoder for the baseband Manchester is illustrated above, where the product block and the integrate and dump make up the corellation receiver for the Manchester code.

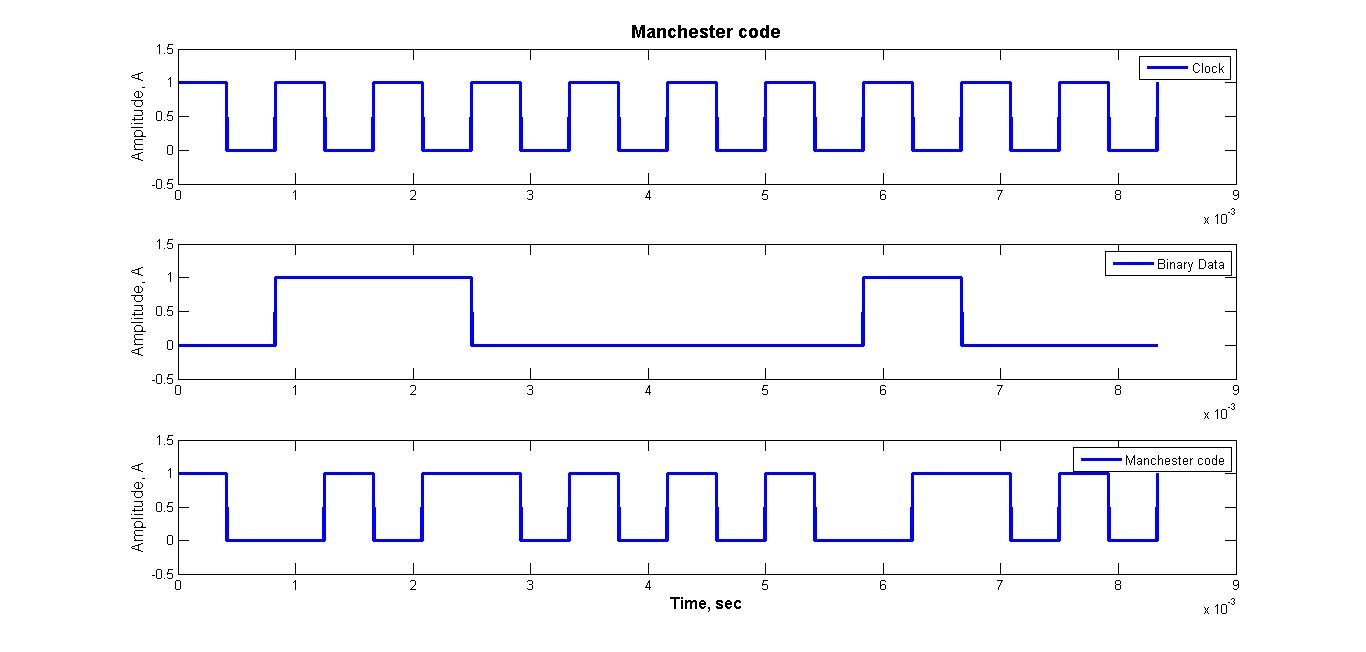


Figure # + 3: Results of the Manchester code

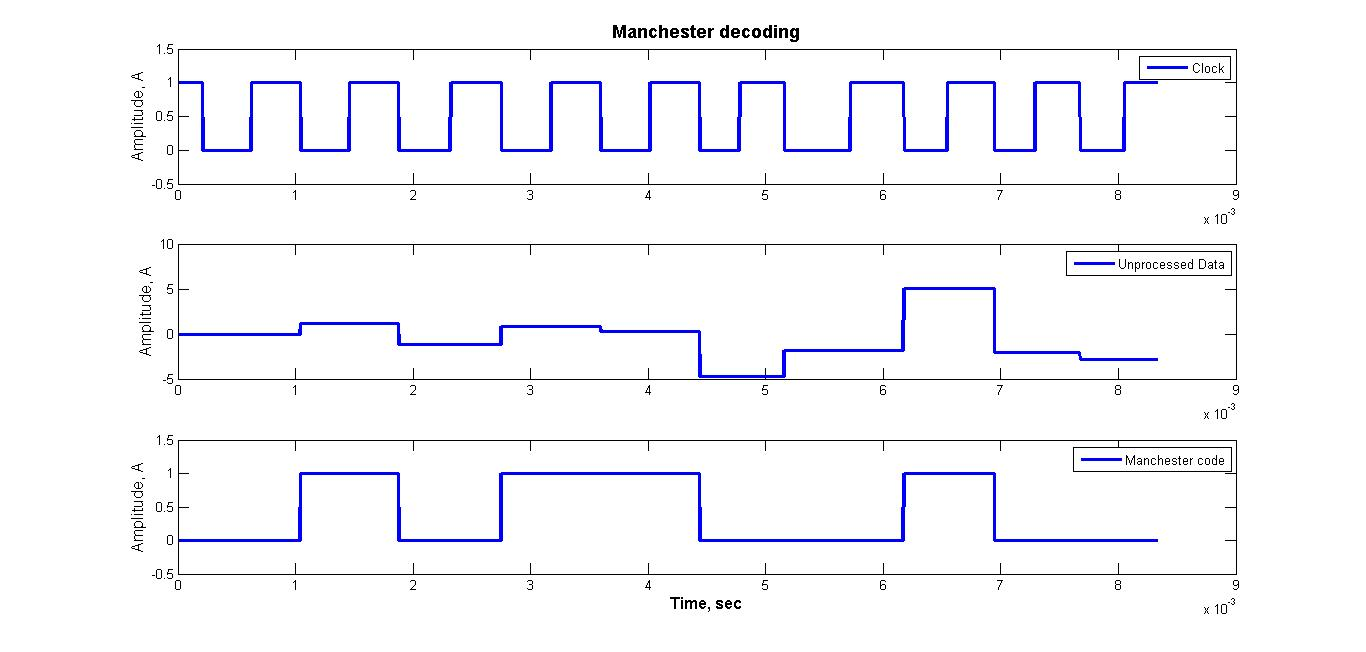


Figure # 4: Results of the Manchester decoding

### Modulation of FSK and BPSK

In PSK, each bit corresponds to a distinct phase of a sinusoidal carrier. For BPSK, these phases are chosen to be 0 and 180 degrees with the transmitted signal, represented mathematically as shown in equation (6).

Then exploiting the fact that, the expression for the transmitted BPSK can be re-written as:

where is the Amplitude and is the carrier frequency of the transmitted BPSK signal. From equation (7), the Simulink model of the BPSK modulator can be designed to gate two antipodal sinusoidal carriers with and. This implementation is illustrated by the Simulink model in Figure 12.

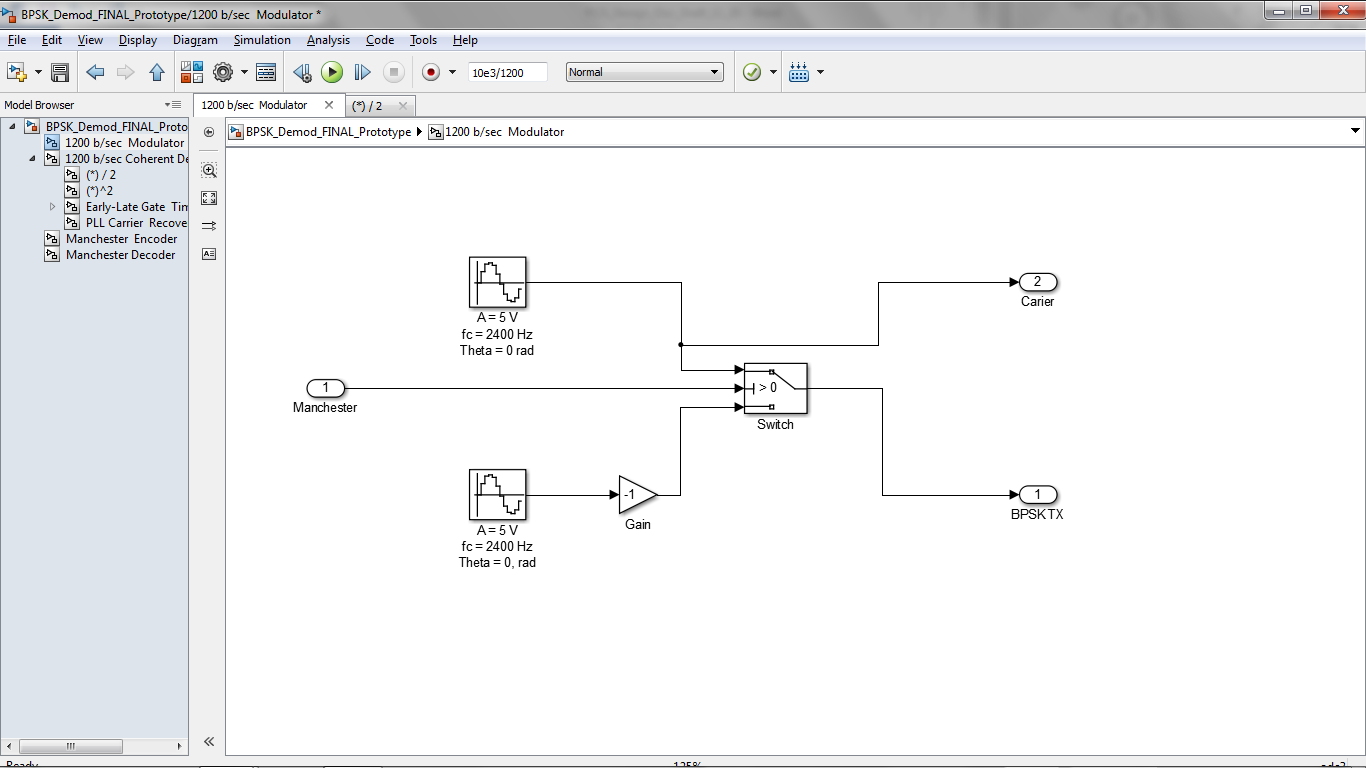


Figure 12. BPSK modulator that uses the Manchester data stream to gate two antipodal sinusoidal carriers that result in the BPSK modulated signal.

Figure 13 below presents one particular simulation that illustrates the operation of the BPSK modulator.

When the input Manchester code is ‘high’, the positive sine wave is transmitted and when the input is ‘low’, the negative sine wave is transmitted.

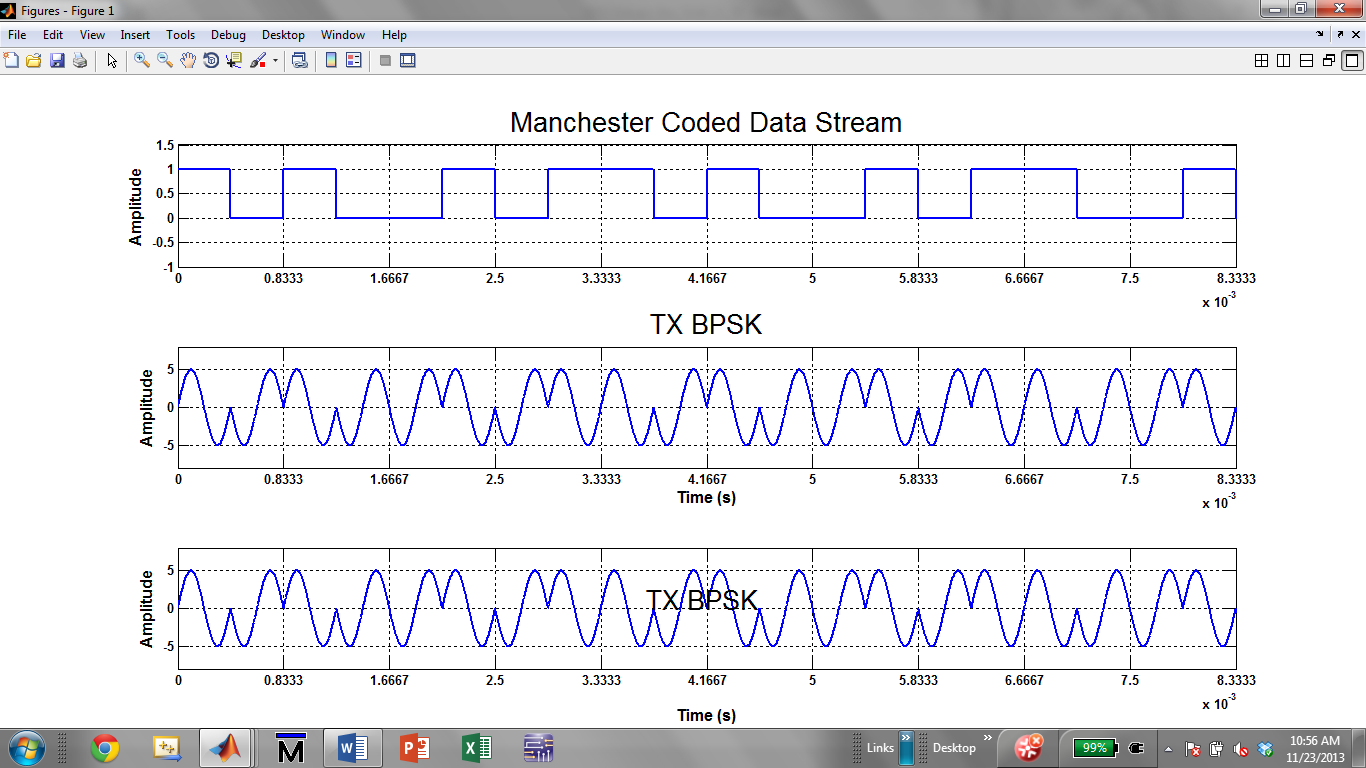


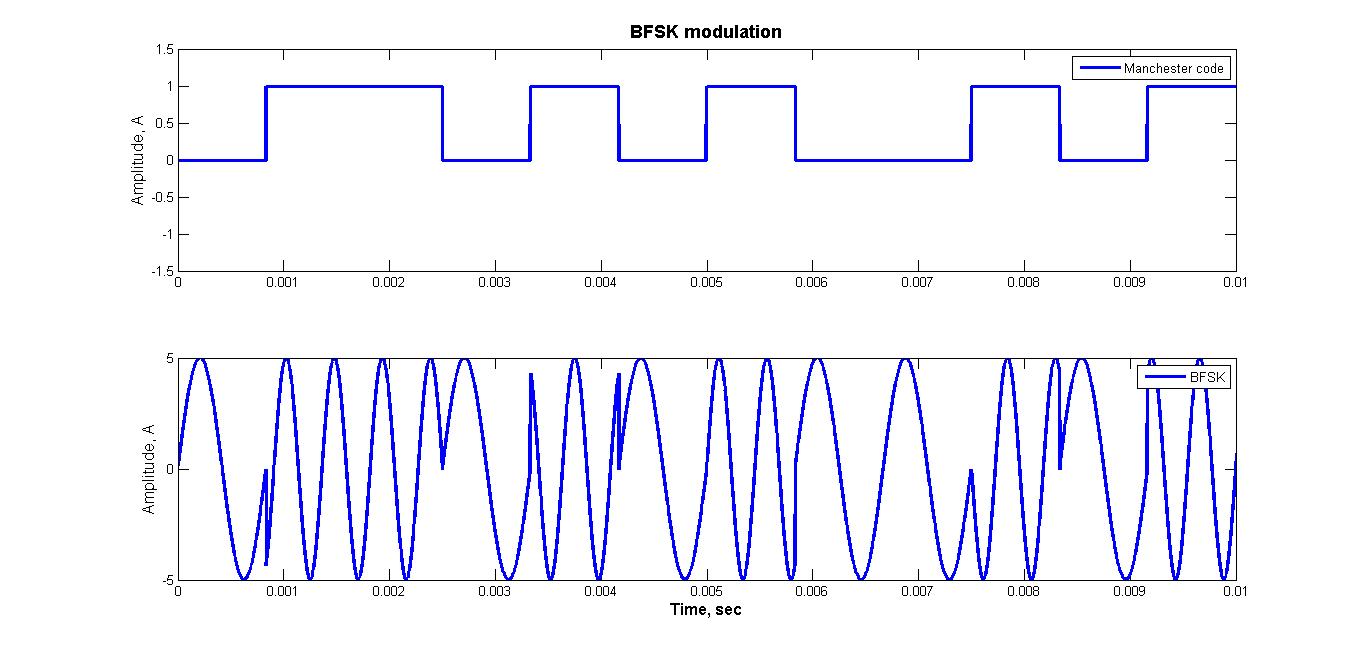
Figure 13. The transmitted BPSK signal has 180 degree phase shifts that correspond to logic level transition of the Manchester coded data stream.

**FSK Modulation**

FSK Modulation may be implemented either coherently or non-coherently where the linearity between the tones dictates the type of modulation. The non-coherent modulator which is the simpler of the two is obtained by simply gating the mark and space with the Manchester coded waveform. Therefore the multiplexer of Figure # - 4 can be used to obtain the behavior of the non-coherent modulator. In Simulink, the modulator is obtained using a switch to let through the tone corresponding to the data transmitted. The signal is described to have a random phase () modeled as a uniform random variable from at the start of the bit time. Although non-coherent modulation may yield the lower error probability, engineers have favored the non- coherent modulator because of its simplicity and lack of complicated analog components (Wilk, 1995.) Therefore, the FSK modulation has been represented using the following equation to illustrate the relation between the phase and the frequency shift.

By directly gating two different frequencies an FSK signal is generated according to the Bell 202 protocol which states:

The Bell 202 protocol can be illustrated using Figure #, which is obtained in Simulink using the switch illustrated in Figure #, bottom



Machine generated alternative text:
Switd,

Figure #: BFSK non-coherently modulated using switches

### Coherent Demodulation of FSK and BPSK using Phase Lock Loops

**PLL Design for Coherent FSK Demodulation**

In every communication system demodulation is an essential element to complete the system. Recovering the data is done either coherently or non-coherently depending on the technic us to modulate the two frequencies. Because the receiver has no information on the transmitted data (in terms of the phase) the receiver must consider the transmitted phase of the transmitted signal. The non-coherent demodulator of Figure # ignores the phase of the signal using two branches to demodulate. The non-coherent demodulator is implemented only with filters, therefore can be easy to implement in terms of setting and adjusting the filters (Mark - 2200 Hz and Space 1200 Hz.) However, inter-symbol interference is certain to occur which will complicate the demodulation process at the receiver. Hence the demodulator of the BFSK modem will consist of a coherent demodulator using a PLLL to keep track of the random phases the signal may undergo. As discussed by (Lindsey et al) the PLL estimates the frequency of the frequency of the signal and outputs the correlation between the tone and the running frequency of the VCO.

To include the PLL onto the modem, the non-linearity of the PLL was modelled around its three components the Phase detector, the Loop Filter, and the VCO. The PLL is then made linear with the assumption that the phase difference between the transmitted signal and the output signal from the VCO is small. Then the PD which is implemented using a multiplier approximated to be only the difference between the signals with a gain KD and then passed through a loop filter with wide enough to pass the modulated frequencies. The output of the loop filter is taken as the demodulated FSK and fed back to drive the VCO.

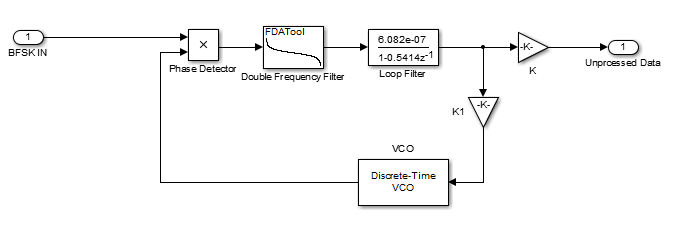


Figure #: Model of the PLL for BFSK demodulation in Simulink

In the demodulator, the output of the loop filter is the demodulated FSK signals, analyzing the PLL, using basic modeling technics the system can be simplified to a single transfer function. The transfer function of the linearized PPL model is used to optimize the demodulation using basic controls concepts. The loop filter can be implemented in several different methods either lead-lag, active filters or a simple low-pass filter. In our BFSK modem, the loop filter was designed using the low-pass filter because of the PLL FSK demodulator's frequency response. Therefore the PLL is modeled by the following equation:

Where is the transfer function of the desired Loop filter. Then replacing with the transfer function of a Low pass filter yields the desired transfer function of the FSK PLL.

Second order transfer functions are often represented using the mechanical terms ζ, the damping ratio and ωn the natural frequencies.

Optimizing the system in terms of the settling time we see that the loop filter must have a wide bandwidth

to obtain an appropriate settling time since:

Therefore, the cut-off frequency of the low-pass filter was set at frequency 20 times greater that of the   
bit rate:

The parameters of the equation are found as follow:

Where the damping ratio is chosen to be = 0.707, and the natural frequency is calculated to be:

A step response can be done to evaluate the parameters of the design. Where a step on the system corresponds to an abrupt change of frequencies, while the bode plot of the system is illustrated in the Figure # + 1

Machine generated alternative text:
80
75
70
65
co 60
C)
t
D 
4-D
C
a’
50
45
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30
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Bode Diagram
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j
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j
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jijj••••••••j•••••
10’
1
Frequency (radis)
1
1

Figure # + 1: Bode plot of the PLL for FSK demodulation

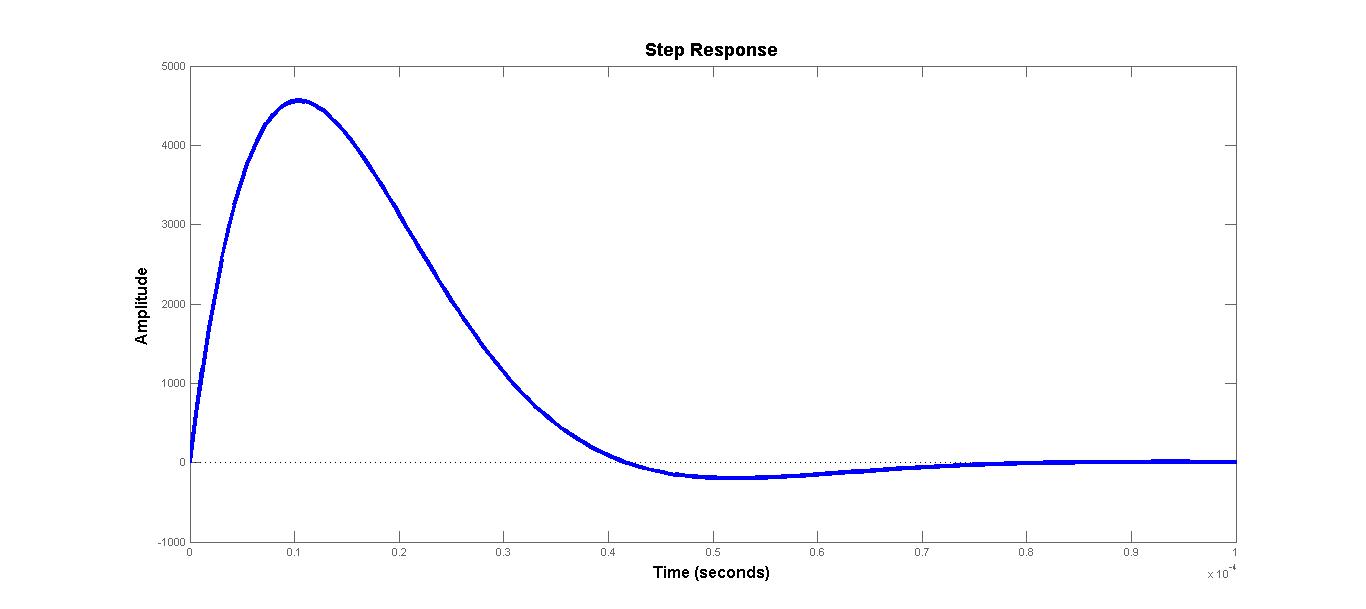


Figure # + 2: Step response of the PLL for FSK demodulation

The completed PLL can then be included into the BFSK demodulator using a discrete VCO, a multiplier for the phase detector and a loop filter. The demodulated data then passed to an envelope detector to further process the data and is finally recovered using the Early-Late Gate method for data recovery.

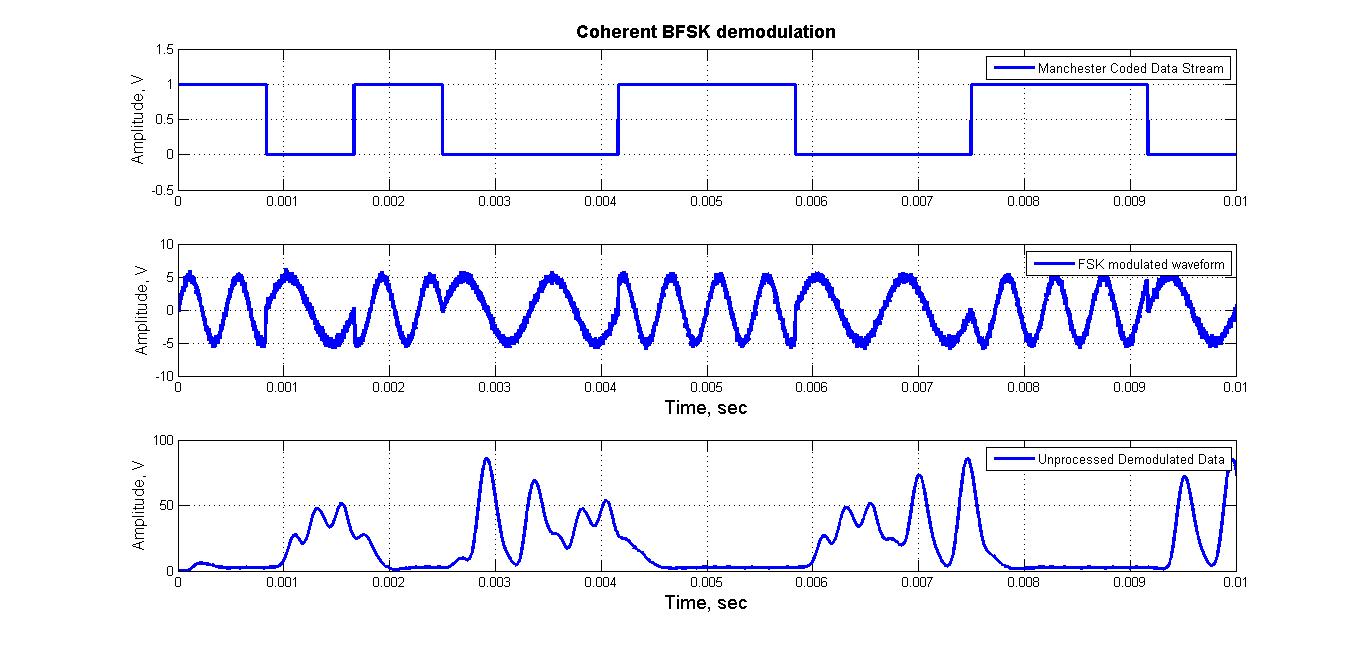


Figure # + 3: Unprocessed data from the PLL Coherent demodulator

**PLL Design for Coherent BPSK Demodulation**

The Simulink model of the squaring loop demodualtor that was introduced in section 1 is shown in figure 14. The received signal is first passed through an IIR peaking filter with a single peak at 2400 Hz and a bandwidth of 10/. This corresponds to the fifth null bandwidth of the BPSK signal and the point in which 98% of the total power is captured (Silage, 2009). This filter acts to remove as much noise as possible without loss of information.

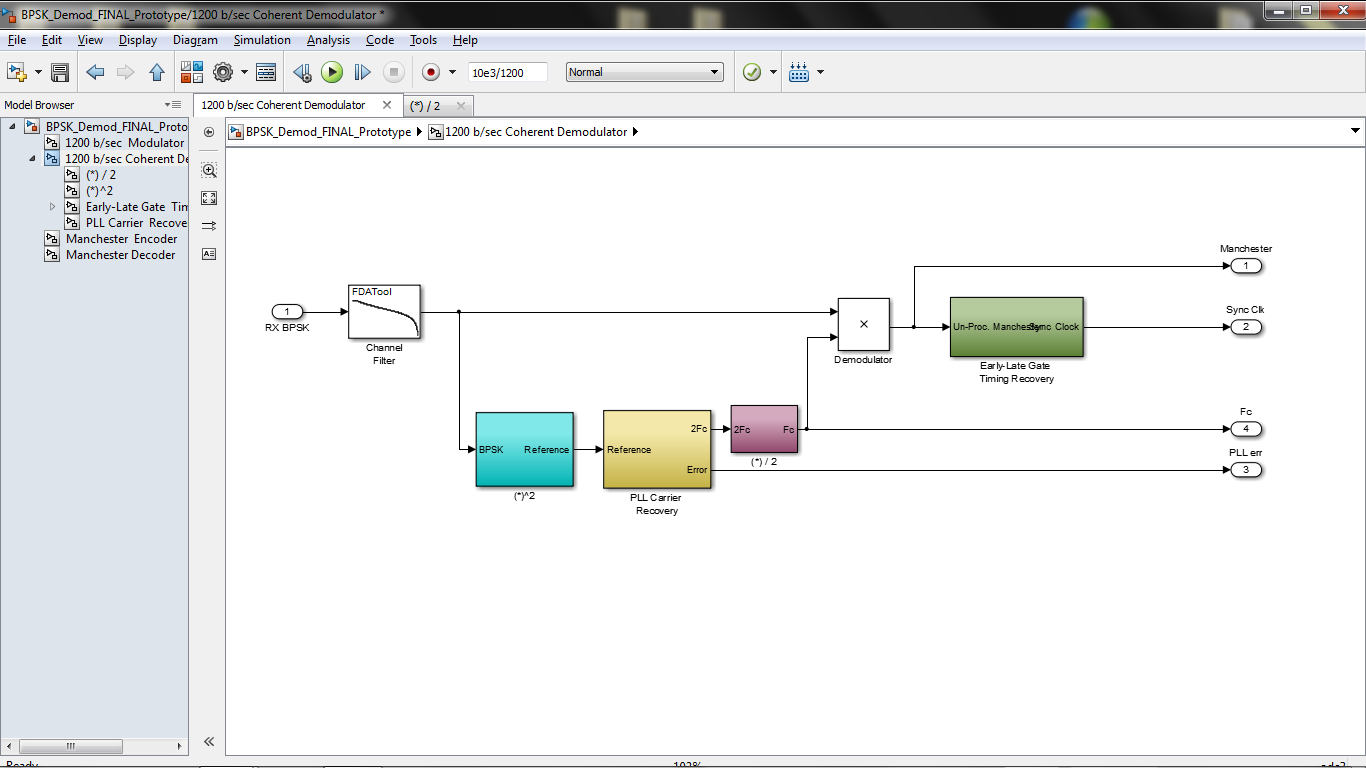
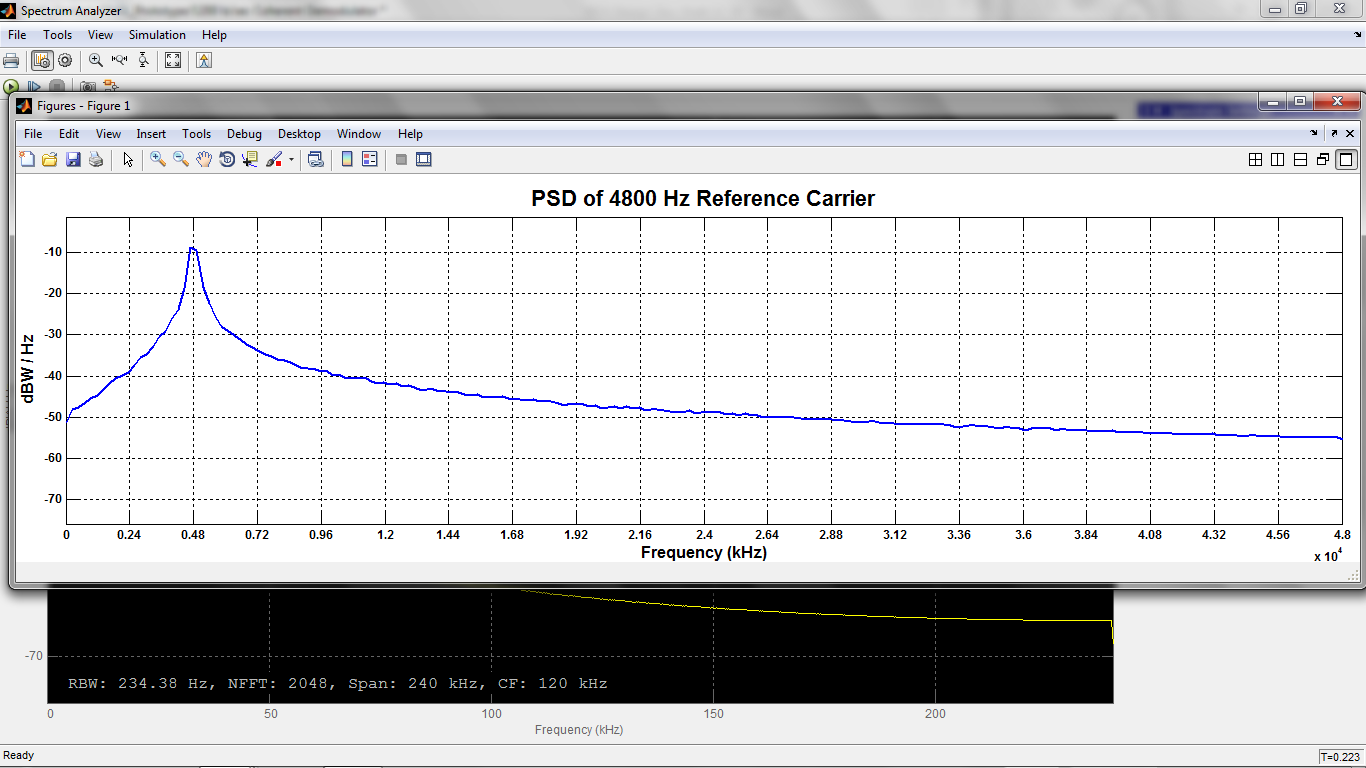


Figure 14. Simulink model of the Squaring loop Demodulator. The carrier of the received signal is reconstructed using a PLL where it is used for coherent demodulation. The early-late circuit regenerates the clock for symbol timing.

Unlike FSK and ASK where the received signal contains a spectral component at the carrier frequency for the PLL to lock onto to, the PSK spectral component of the carrier is suppressed within the PSD of the received signal. The solution to this problem is to square the received signal which produces a spectral component at (Nguyen & Shwedyk, 2009). This is easily shown using trigonometric identities. If the received signal is where is AWGN, then,

The DC component and the noise in equation (3) are filtered using a narrow bandpass filter with a center frequency of and a Q of 100. The resulting PSD after squaring and filtering is displayed in Figure 15.



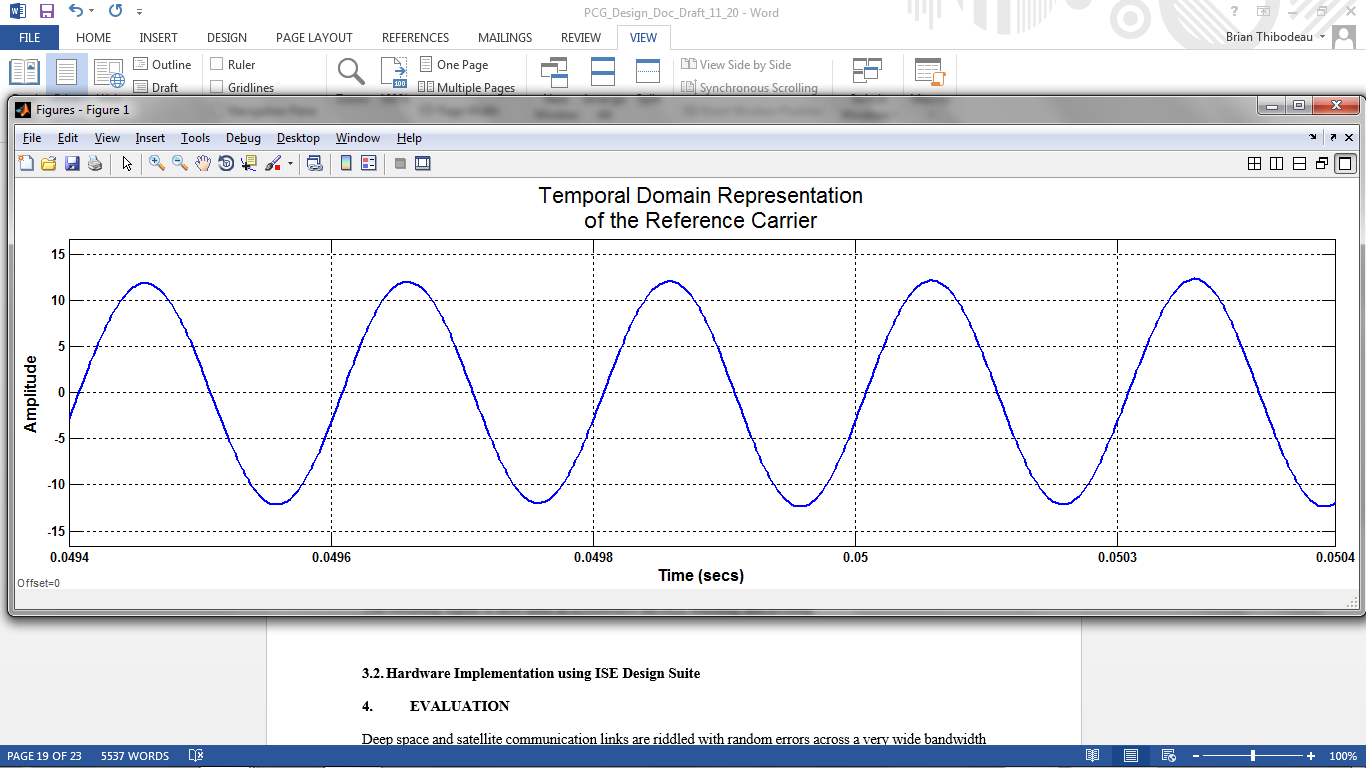


Figure 15. (Top) Power Spectral Density of the 4800 Hz reference carrier and (Bottom) the temporal domain signal of the reference carrier

The reference carrier is shown on the bottom of Figure 15 and is forwarded to the PLL where the phase and frequency of the reference carrier is estimated.

**Phase and Frequency Estimation using a PLL**

All PLL’s are composed of three components, the phase detector, loop filter, and the VCO. Its operation can be understood by considering the PLL in figure 16. The Phase detector includes the multiplier, phased detector gain and filter. The reference carrier at is multiplied by the locally generated sinusoid which after low pass filtering at produces the phase error. Note that the PLL analysis assumes that the reference frequency is approximately the same as the VCO frequency. Any minor differences are considered in the phases and of the reference and VCO respectively (Nguyen & Shwedyk, 2009).

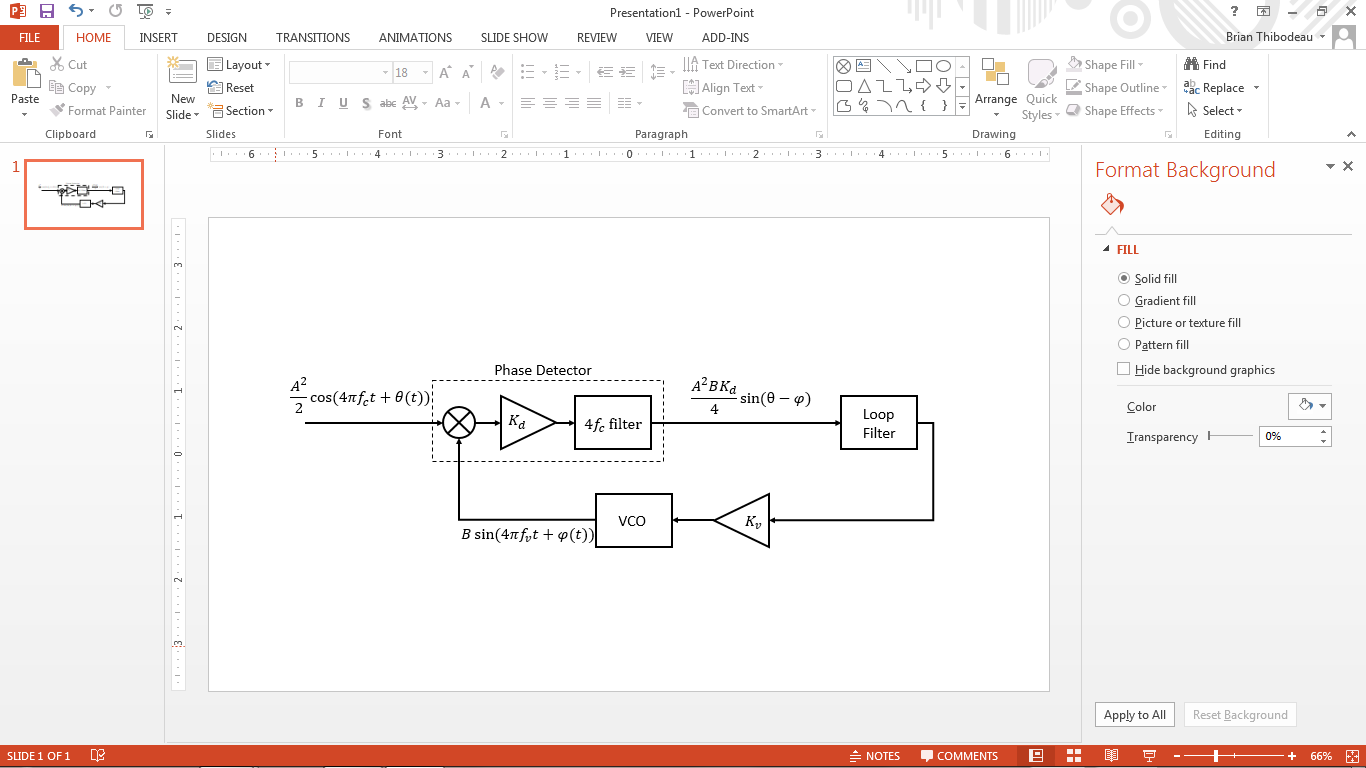


Figure 16. Time domain model of the PLL used for carrier frequency and phase estimation

The multiplication in the phase detector makes the PLL highly non-linear, but if the phase error, , is small than the output of the phase detector can be approximated as, . Under this approximation, the linearized PLL in terms of the phase is shown in Figure 17.



Figure 17. Linearized PLL in the Laplace domain. Note that the filter is omitted in the linearized Laplace model because it is assumed that the double frequency component was filtered leaving only the phase error

Once the PLL has been linearized by making the assumption that the phase error is small, conventional controls system theory can be applied. Thus the closed loop transfer function of the PLL in figure 17 is given by,

And the steady error transfer function is,

In order for the PLL to be capable of tracking a phase and frequency step, the appropriate loop filter *L*(s)must be chosen such that steady error transfer has zero error for step () and ramp () inputs. This is accomplished by application of the final value theorem to equation (15). This results in the following:

The results of the final value theorem imply that the loop filter must contain an integrator so that the error at infinity goes to zero. Two common loop filters that accomplish this are the lead-lag filter and the proportional integral filter (PI). In this design, the PI filter was chosen which takes the form,

Where is the proportional gain and is the integral gain. After substituting the loop filter expression into the closed loop transfer function given by equation (16), the new closed transfer function describing the PLL’s behavior is,

Recognizing that equation (17) is a prototypical second order transfer function, the PLL transfer function can be re-written in terms of the natural frequency and the dampening ratio (Crawford, 2008).

Where,

Using the above results, two Simulink models were developed for the design and analysis of the PLL that will be used for phase and frequency estimation in the carrier recovery circuit. The first model is the time domain model that will be implemented in hardware and the second is the linearized model to demonstrate that equations 18, 18.1, and 18.2 can be used to approximate the response of the time domain model.

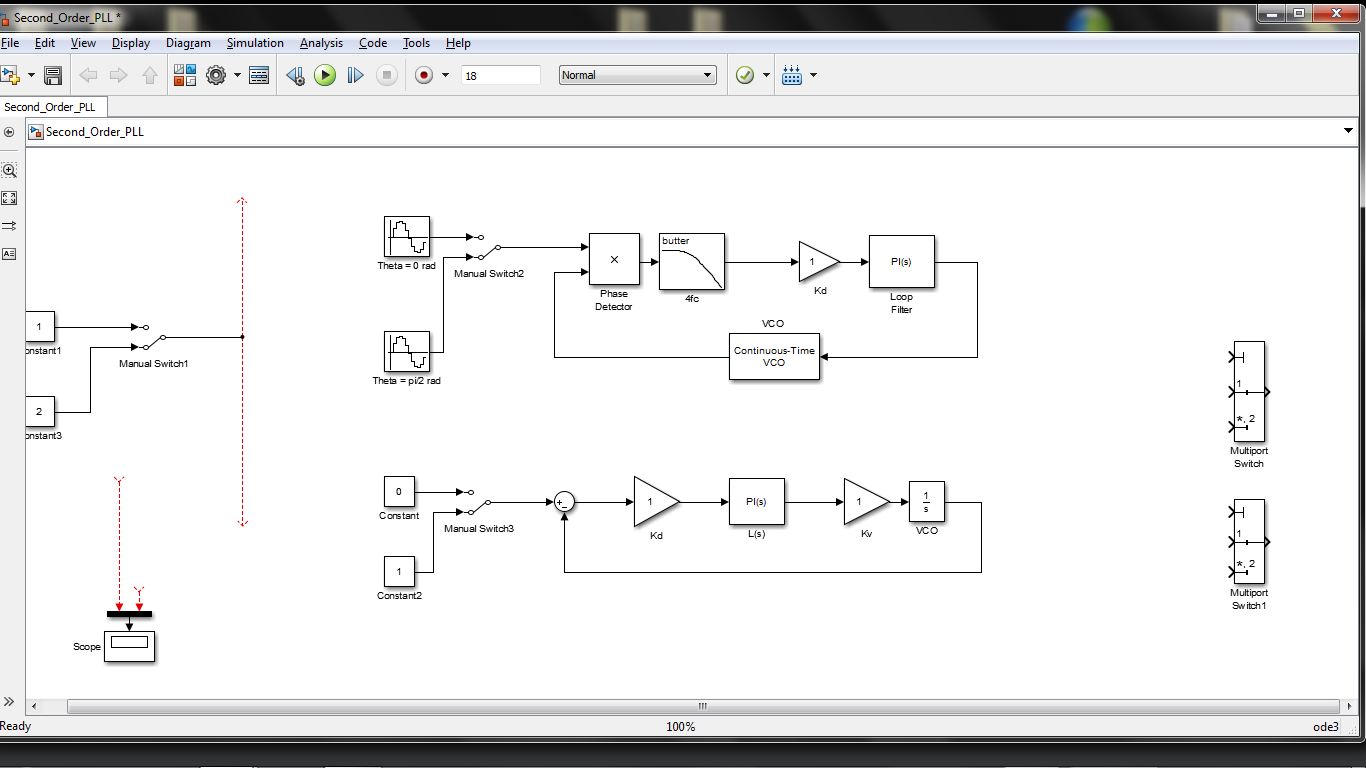


Figure 18. (Top) Time domain model of the PLL used in the carrier recovery circuit and (Bottom) linearized PLL.

The BPSK modem is designed to operate at 1200 b/sec in order to meet the requirements of LEO-AMSATS. Because of the possibility of sudden phase shifts due to AWGN in the channel, the PLL must be designed to respond quickly to these changes. Thus the PLL requires a settling time less than ms in order to minimize the number of bits lost during acquisition. From classical control theory, the settling time of a second order underdamped system can be approximated as . If the dampening ratio, is chosen to be 0.8 so as to minimize the overshoot, it can be shown from equations 9.1 and 9.2 that the natural frequency, should be 6000 rad/s. The resulting phase detector, VCO, proportional and integral gains that satisfy the requirements of the settling time and dampening ration are listed in Table 4.

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |
| 1 | 1 | 9600 |  |

Table 4. Phase detector, VCO, proportional and integral gains

In order to verify that the desired settling time is achieved, the gains in Table 4 were appropriatly substitued in the Simulink models illustrated in Figure 18 and simulated. Note that the time domain model simulated a phase step by using two sine wave blocks with one having a 90 degree phase shift with respect to the other. Both had unity amplitude and a frequency of 4800 Hz. The 4800 Hz frequency represents the squared reference carrier that was discussed earlier. The low pass filter in the phase dectector is first order with a cutoff frequency 9600 Hz.

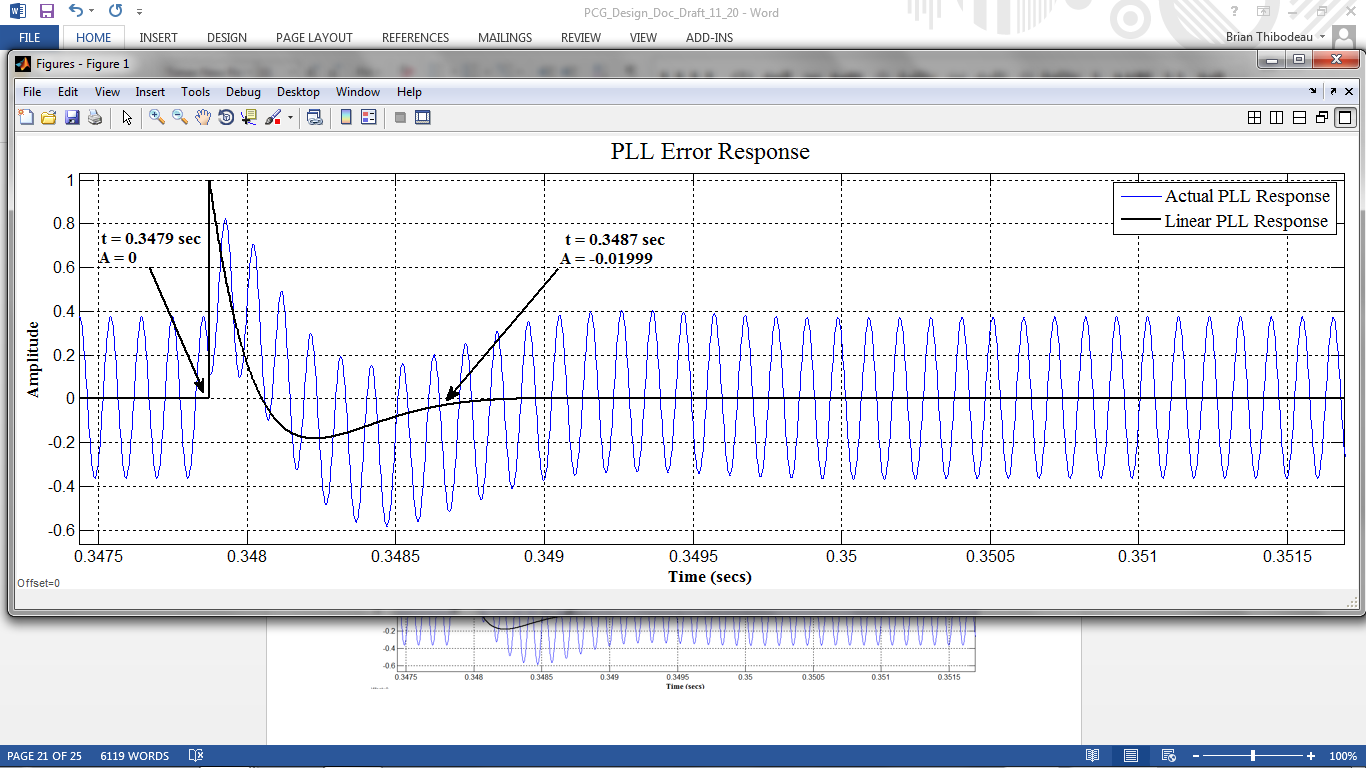


Figure 19. Comparison of the actual PLL error response to the linear PLL response

In figure 19, the blue sinusoidal response is the actual PLL response to a phase step while the solid black line is the error response of the linear model. The step occurred at and reached 2 percent of its final value at resulting in a settling time of 0.8 ms. It can be seen that the linear PLL response closely approximates that of the actual PLL response. Lastly, the PLL was subject to extreme case of a 4800Hz frequency step. This is twice the frequency of the nominal reference carrier. As illustrated by Figure 20 below, the PLL still manages to lock onto the reference carrier. It does so at the cost of long acquisition and lock time. The time to lock in the extreme case of a 4800 Hz frequency step is approximately 15.8 ms. Although it’s unlikely the PLL will be subject to such large frequency steps, it demonstrates the robustness of the design.

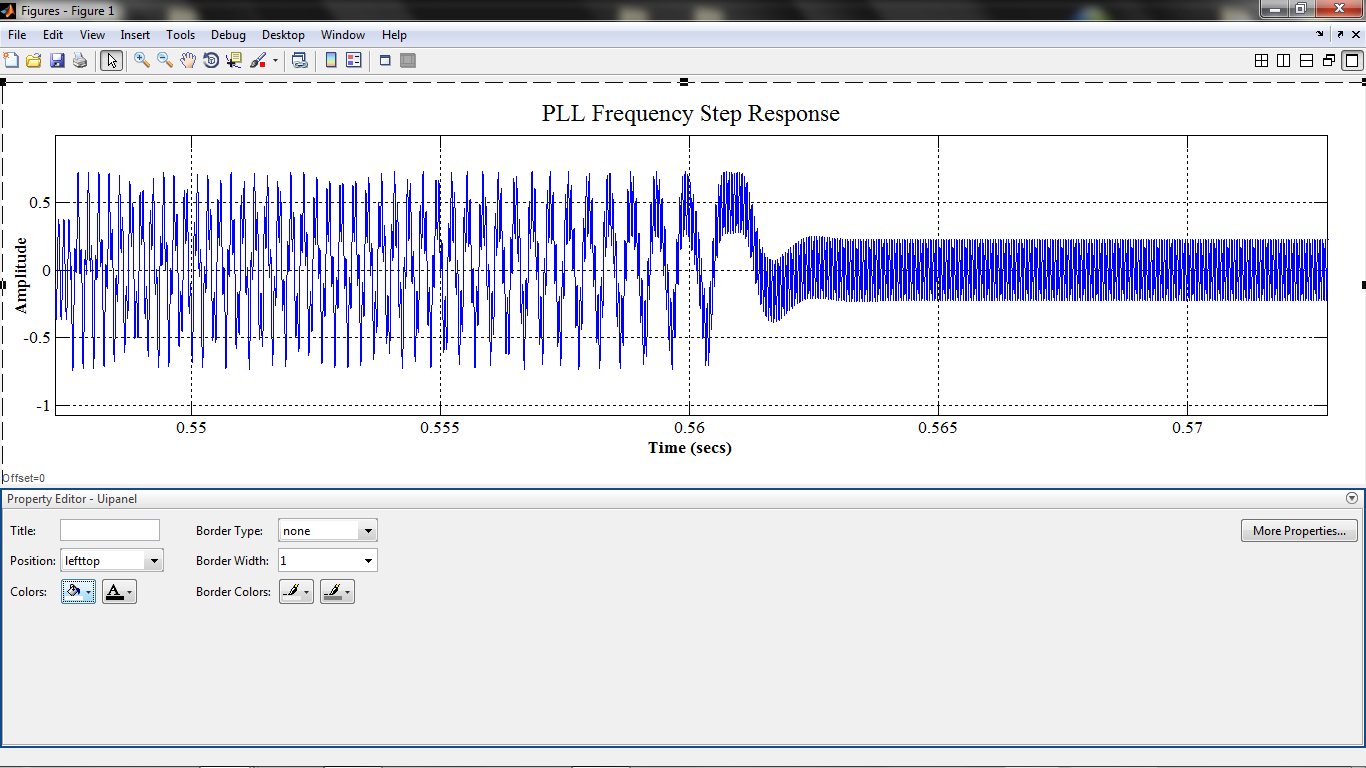


Figure 20. PLL frequency step response to a 4800 Hz step. Time to lock after frequency step is approximately 15.8 ms.

After the PLL locks onto the reference carrier, the output is taken from the VCO which is at twice the frequency of the transmitted carrier. Dividing the VCO output by two is accomplished using a D-Type flip configured as a frequency divider. In Simulink this requires converting the output of the VCO to a square wave so it can be fed to the clock input of the D-flip flop. The output of the D-flip flop is pass through a narrow bandpass filter with center frequency of 2400 Hz and a Q of 10. Figure 21 compares the 4800 Hz square wave from the PLL to the output of the divide by two flip flop.

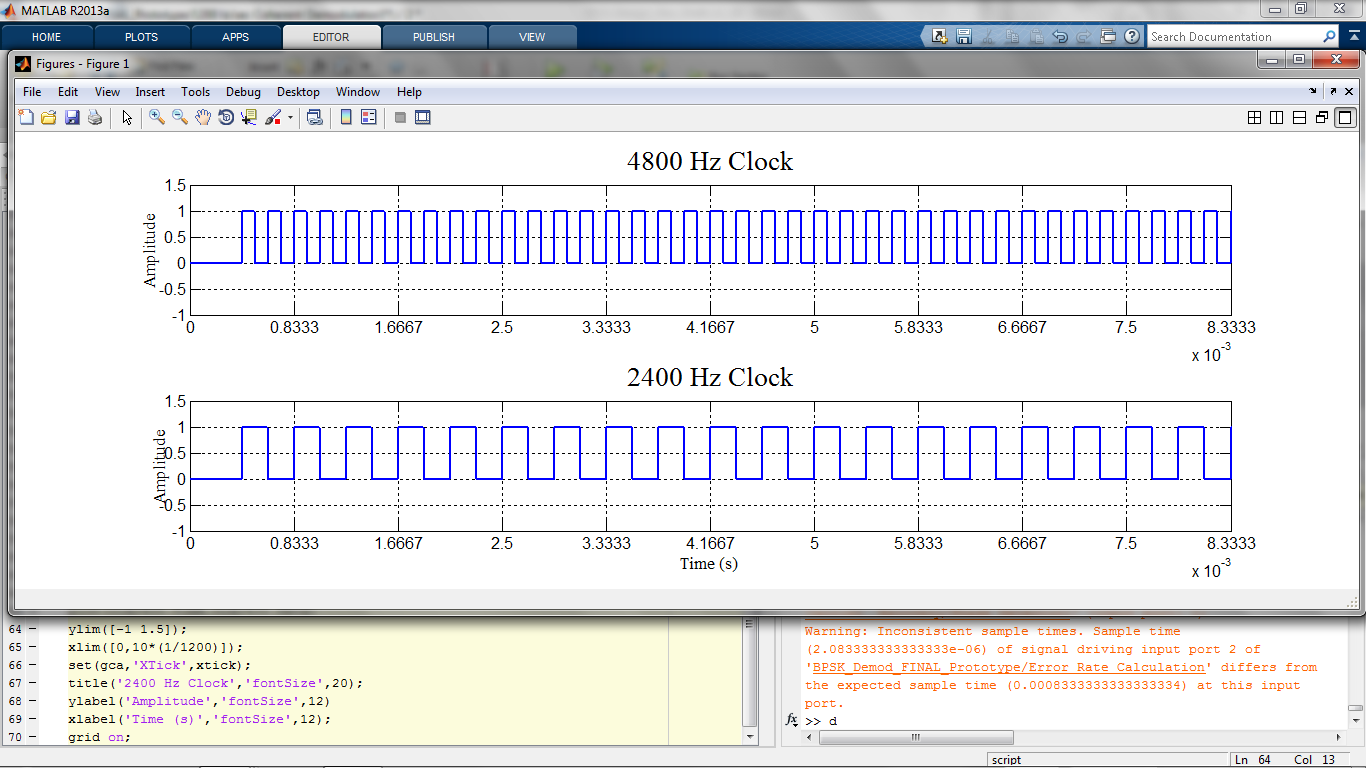


Figure 21. (Top) 4800Hz carrier reference from the PLL after being converted to a square wave. (Bottom). 2400 Hz in phase carrier following the divide by two flip-flop.

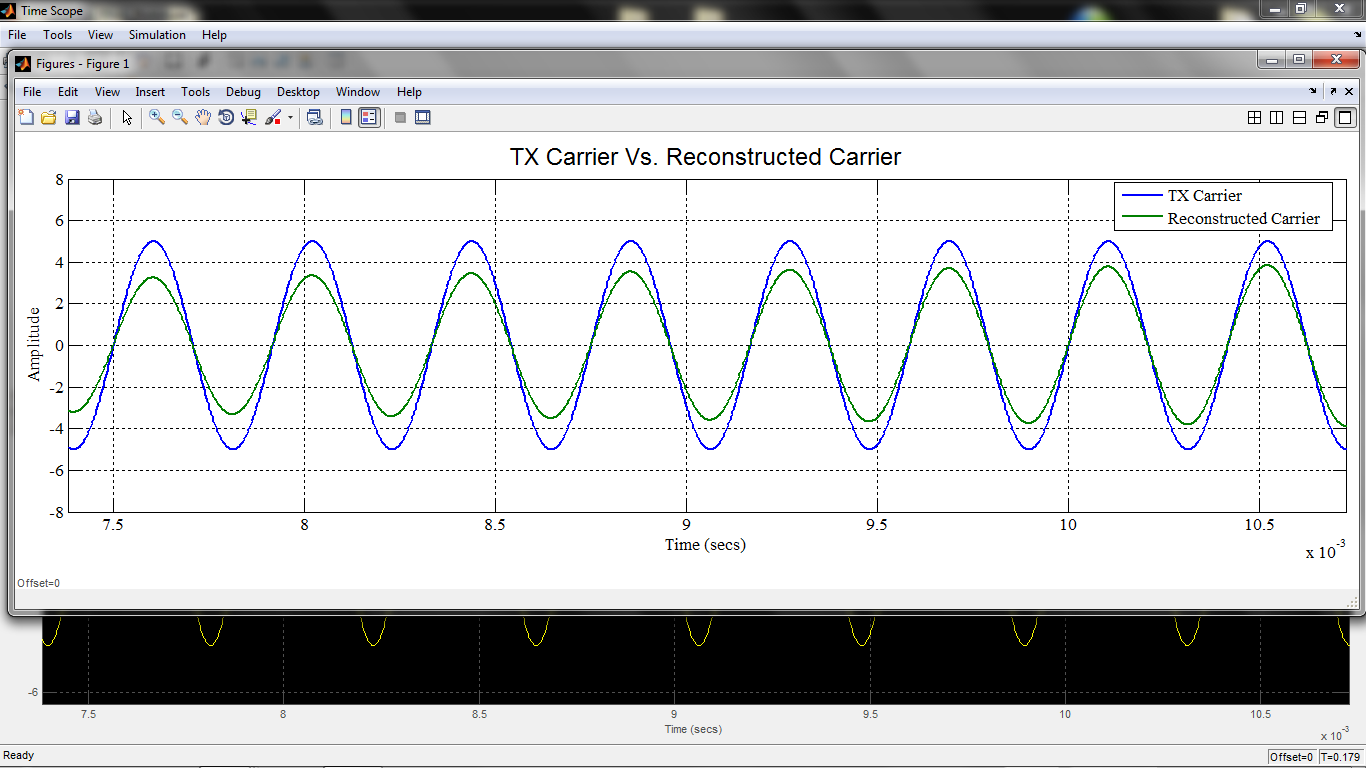


Figure 22. Transmitted carrier superimpose onto the reconstructed carrier demonstrating the PLL’s ability to track the phase and frequency of the received signal.

**Timing Recovery Using Early-Late Gate Synchronizer**

Once the carrier is reconstructed, it is sent to the correlator where it is mixed with the received BPSK signal. The output of the multiplier is the sampled baseband data that must be sampled at the appropriate time in order for correct symbol determination. This is accomplished by extracting a clock from the recovered baseband data. This process was made easier by the Manchester encoding that took place in the modulator. Figure 23 illustrates the Manchester data recovered from the mixing of the BPSK signal and the reconstructed carrier.

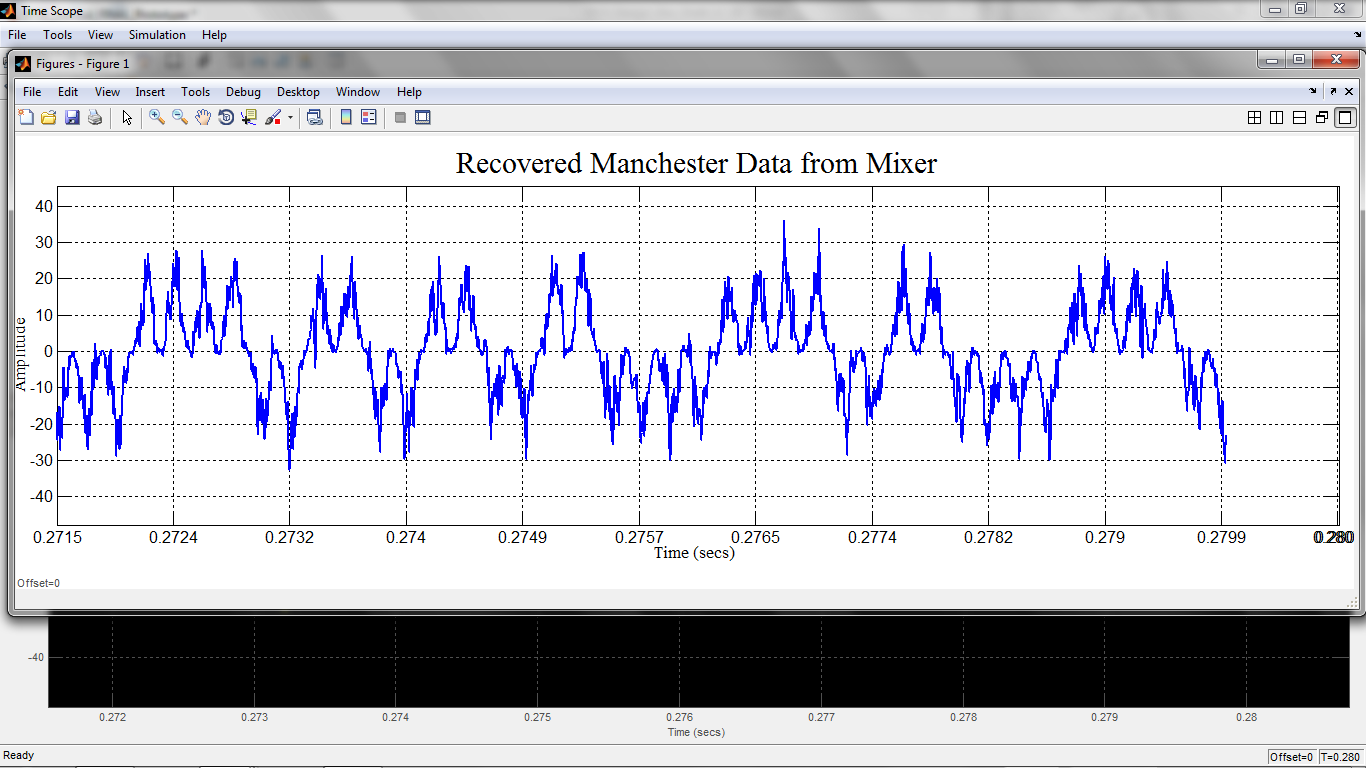


Figure 23. Reovered Manchester data that is forwarded to the early late-gate synchronizer for clock extraction.

The method that was chosen for timing recovery was the closed loop early-late synchronizer. This is a closed loop feedback system similar in operation to a PLL. It continuously tracks and adjusts a local oscillator until the output clock is synchronous with the recovered Manchester data. Its operation is can be explained more clearly by considering the Simulink model of the Early-Late gate circuit.

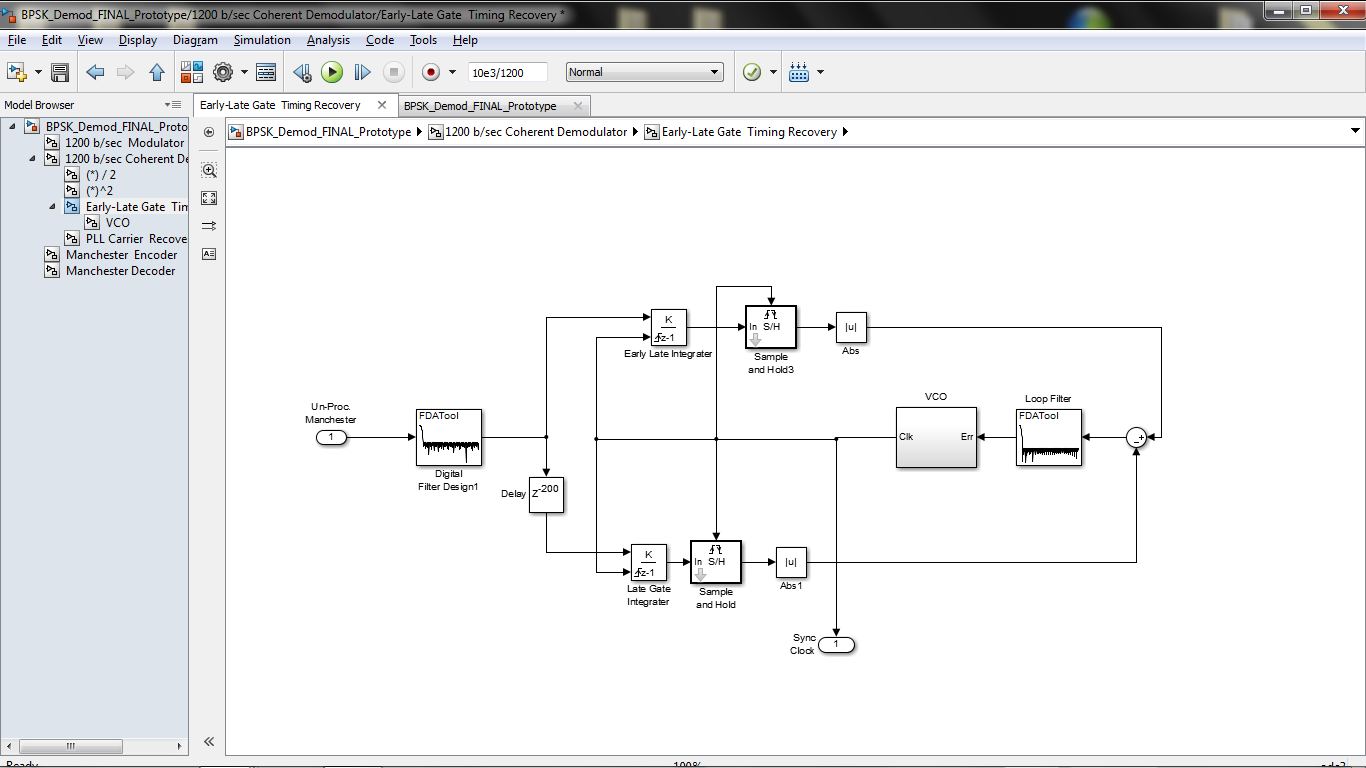


Figure 22. Early-Late Gate synchronizer used for clock extraction

A low pass filter is placed before the Early-Late gate synchronizer so as to minimize the amount of noise in the circuit. The sampled Manchester data takes two paths after being low pass filtered, the first is the early gate branch (top branch) and the second is the late gate branch (bottom branch). The early gate branch starts accumulating energy on the rising edge of the VCO clock and is sampled at the falling edge. Conversely, the late gate branch begins accumulating energy on the falling edge of the clock and samples on the rising edge. Both the early and late branches rectify the samples thus producing positive voltages so that an error signal is derived when the two branches are subtracted.

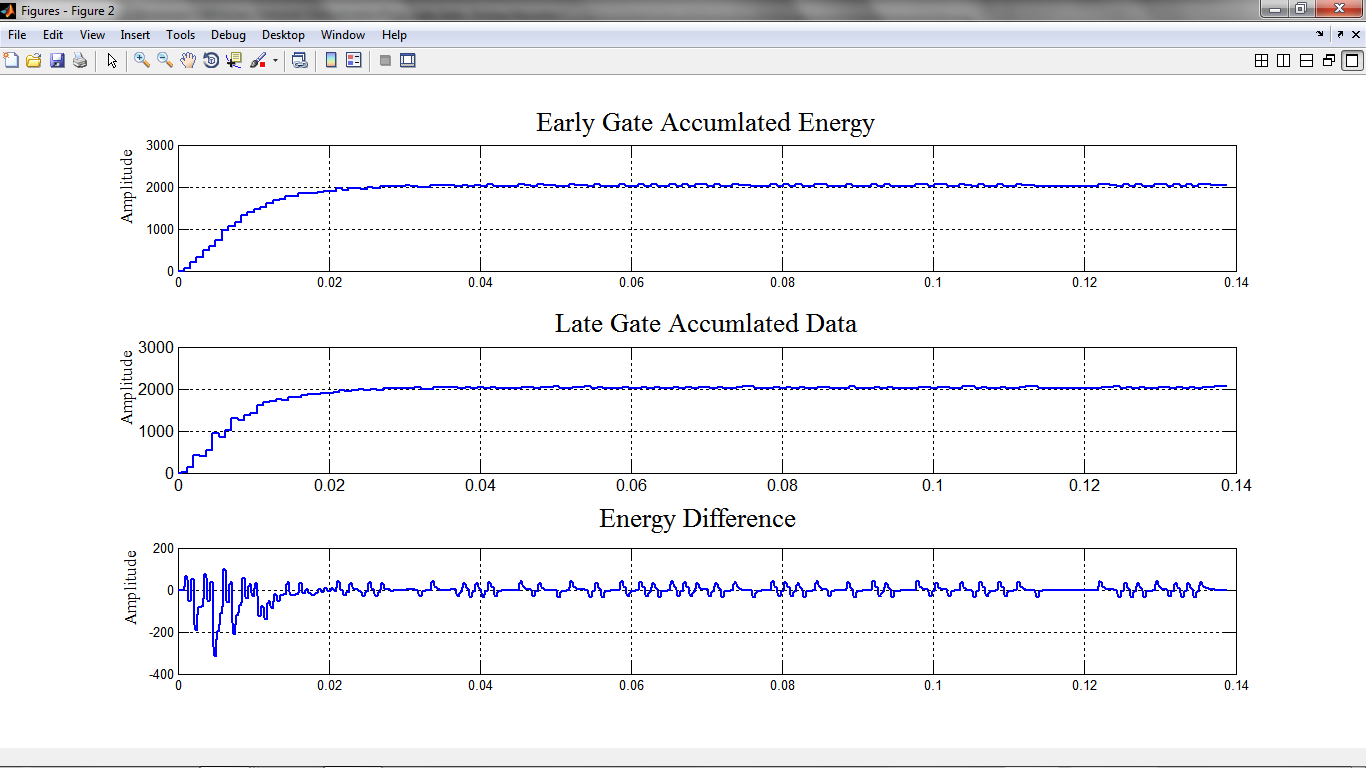


Figure 23. Energy accumulated from the early compared to the energy accumulated from the late gate. The difference in accumulated energy between the early and late gate is used to drive the VCO towards a synchronous clock

Figure 23 depicts the accumulated energy of the early and late gate branches in a addition ot the error signal that feeds the VCO. The results show that in the first 20ms the early late gate sychronizer is tracking the received signal. This is indicated by the large energy difference in the bottom plot of figure 23. The transient effect depicted in the accumalted energies in each branch are likely the cause of the start up time of the various filters in the reciever. The output clock of the VCO is compared to the received signal in figure 24 to illustrate the phase coherency. Since this clock is now sychronized with the transmitted signal, it can be used to sample the recovered manchester data in order to make the correct symbol determination. Note that this subsystem is applicable to both the FSK and BPSK modems since they both use the same bit rate of 1200 b/sec.

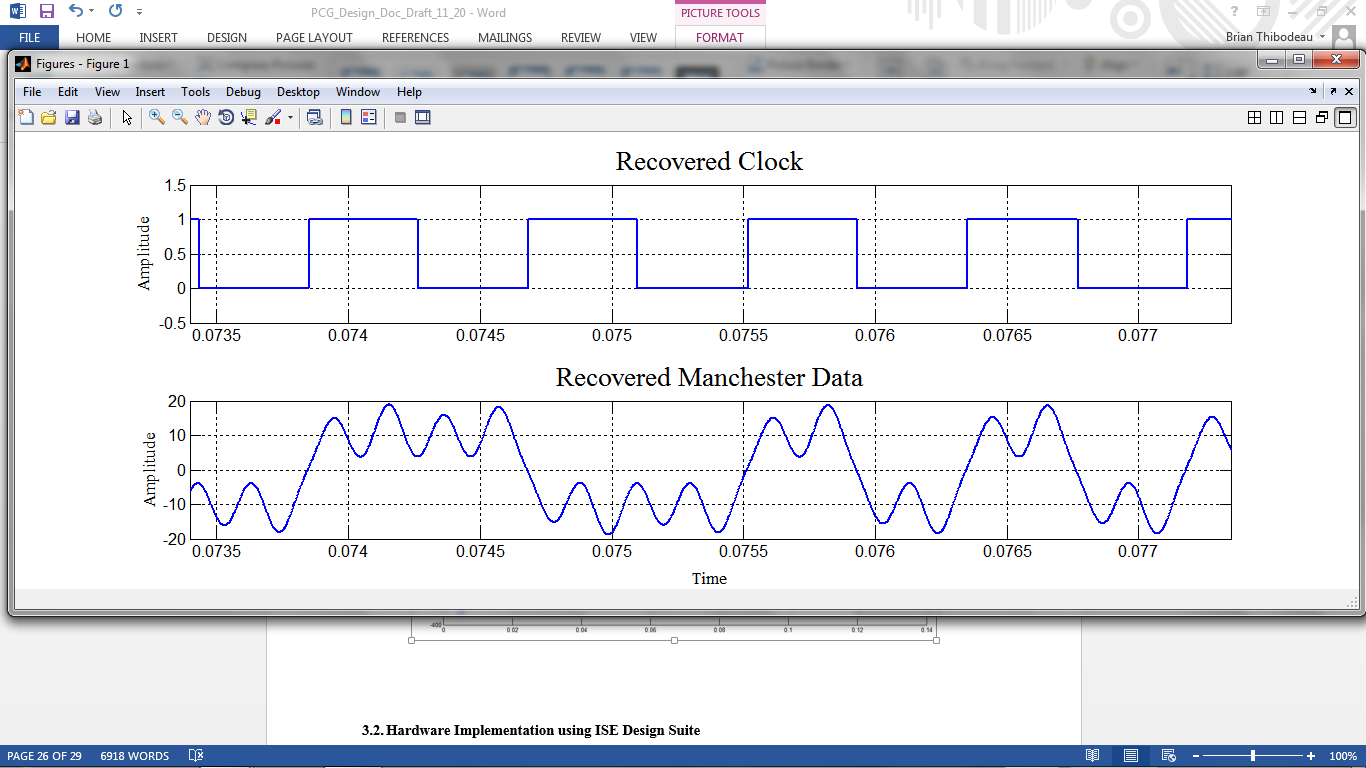
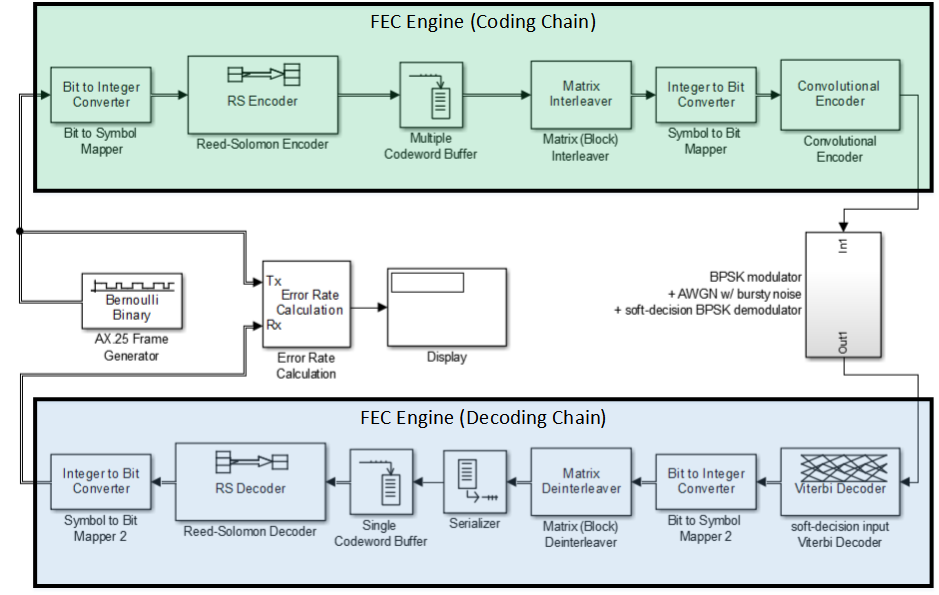


Figure 24. The recovered clock after synchronization is compared to the received Manchester data stream to demonstrate phase coherently

### Concatenated FEC codes (Brandon)

The third digital communication system to be analyzed is System C – which comprises everything in System B with the addition of a forward error correction (FEC) engine and a modification to the BPSK modem. Specifically, the modification includes making the BPSK demodulator implement soft-decision decoding instead of hard-decision decoding. This change will prove to be beneficial to the overall SNR of the digital communication system. An explanation of this will appear shortly as we describe the FEC engine in a clockwise fashion (see Figure 3.1.3.1) starting with AX.25 frame generation (top left) and looping back around to packet error rate calculation (bottom left).

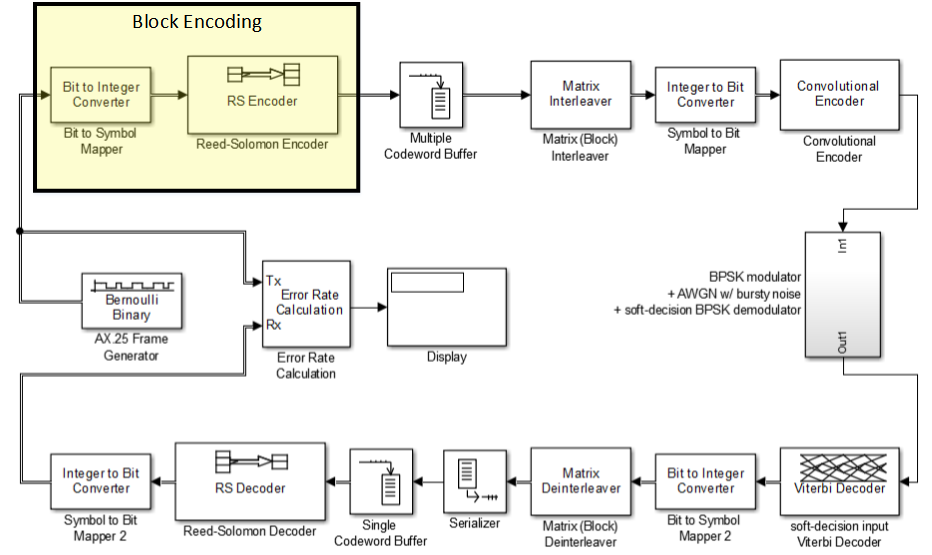


**Figure 3.1.3.1.** A system-level diagram depicting System C with the FEC engine. The engine is comprised of a coding chain and a decoding chain. Besides from the addition of the FEC engine, System C differs from System B in that the BPSK demodulator implements soft-decision decoding instead of hard-decision decoding.

The FEC engine comprises a concatenation of two forward error correcting codes. As discussed in Section 1, one of the codes will be a block code (correcting burst errors) while the other code will be a convolutional code (correcting random errors). The next text segments will elucidate the reasoning for this concatenation of FEC codes.

**Block Encoding** **(and Decoding)**

One of the general categories of forward error correcting codes is *block codes*. Reed-Solomon (RS) codes, one form of block codes, perform exceptionally well in correcting burst errors in a received signal. This senior design project elected to incorporate an RS code into the FEC engine for the sole purpose of correcting burst errors that seep into the received bit stream. Figure 3.1.3.2 highlights the section of the FEC engine dedicated to block *encoding*.



**Figure 3.1.3.2.** Highlights the block encoding unit of the FEC engine.

At this point, one may ask themselves how does block *encoding* work to correct burst errors. To answer such a question, we must understand that once block *encoding* is done, it must be undone at some point – this is block *decoding*. Block *decoding* will be discussed shortly, but let us first examine how block *encoding* works and how we use Simulink to simulate its functionality. It should be noted that this will be a high-level explanation that circumvents the detailed implementation of block coding. Specifically, a thorough description of Reed-Solomon codes requires an involvement of abstract algebra, specifically Galois fields (Sklar, 2001). In this regard, the curious reader is recommended to visit the excellent mathematical treatment provided in the digital communications textbook entitled *Digital Communications: Fundamentals and Applications (2nd Edition)* by Bernard Sklar*.* Additionally, an RS code can be realized using a linear feedback shift register (LSFR), but in the interest of time, this senior design project has elected to utilize intellectual property cores in order to bypass this design step.

Let us first begin the explanation by imagining a bit stream. The block encoder deals with correcting *symbol* errors*,* not single bit errors. For instance, a group of 3 bits could be abstracted to one of eight symbols (0 through 7). This functionality is represented by the *Bit to Symbol Mapper* in Figure 3.1.3.2. The symbol is then operated on by the Reed-Solomon encoding process. This is represented by the *Reed-Solomon Encoder* block in Figure 3.1.3.2. Essentially, the Reed-Solomon encoder attaches a set of parity (or redundancy) symbols to the end of a collection of symbols (known as a message word) (Viswanathan, 2013). A RS code converts *k* symbols (the message word) into a codeword, or *block*, consisting of *k symbol*s. The RS encoder essentially extends the message word with *n-k* parity symbols. This is known as an (*n*, *k*) RS code. The following depicts a (7, 3) RS code which converts a 3-symbol message word into a 7-symbol codeword (*block)*:

🡪 [

The inputted bit stream representation of this would look like the following:

The (*n, k*) RS code has an error-correcting capability (*t*) expressed as (Viswanathan, 2013):

Put differently, the (*n, k*) RS code can correct up to *t* symbol errors in a given codeword. For instance, let us pollute the previous codeword example with symbol errors. The first and second of the matrices below show one and two symbol errors, respectively, that are correctable by a (7, 3) RS code. However, the third matrix shows three symbol errors which is greater than the error-correcting capability of a (7, 3) RS code. Consequently, the code fails to correct the symbol errors in the third matrix.

[ correctable

[ correctable

[ not correctable

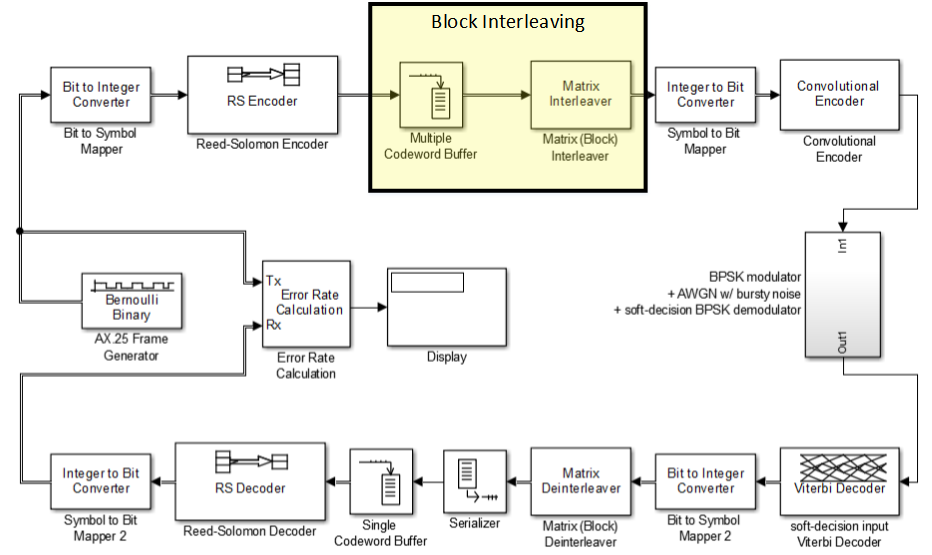
We see that regardless of if one or two symbols were received in error, the (7, 3) RS code could correct the symbol errors. One can imagine a lengthier RS code, such as the (255, 235) RS code, possesses an even more lenient error-correcting capability. In other words, the (255, 235) RS code can correct up to 5 symbol errors within a codeword. If the (255, 235) RS code deals with 8-bit symbols, this means that up to five contiguous symbol errors (up to 40 contiguous bits) are correctable. This elucidates the power of RS codes in correcting for long strings of received symbol errors (burst errors) caused by bursty noise in a propagation medium.

The performance of RS codes are a function of their symbol size (in bits), redundancy, and code rate (Sklar, 2001). One can easily imagine an RS code to be more successful at correcting errors the larger the codeword is, which means that a give burst error is relatively smaller (and hence more correctable). Hence, the larger the symbol size of a RS code, the larger the codeword is, and consequently the better the RS code performs. The code rate of an RS code is the ratio of symbols that comprise a message word and a codeword. Hence, the code rate is expressed as (Viswanathan, 2013):

When the code rate is high, the number of symbols that comprise a message word (*k*) and a codeword (*n*) are fairly close in value. The number of added redundancy symbols is fairly low. Contrarily, when the code rate is low, the number of added redundancy symbols is fairly high. This high number of redundancy symbols equates to a high computational complexity of the RS code and a higher bandwidth requirement (Sklar, 2001). However, a large number of redundancy symbols results in better error-correcting performance. Consequently, this senior design project will aim to optimize the symbol size, redundancy, and code rate for the purpose of increasing error correction capabilities without putting too much demand on hardware or bandwidth resources.

**Block Interleaving (and De-interleaving)**

One can imagine that there are instances where a burst error is too extensive for a given RS code to correct. To increase the chances of the RS code receiving a sufficiently short burst error, we can essentially mix up the codewords from the RS encoder and then transmit the mixed information. This way, when an overly extensive burst error occurs over the propagation medium, the receiver can put the mixed information stream back into un-mixed sequence, which essentially splits the extensive burst error into a disjointed series of smaller, correctable burst errors. This technique is known as *block interleaving*. Figure 3.1.3.3 shows the Simulink blocks of System C responsible for block interleaving.

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**Figure 3.1.3.3** Highlights the block interleaving unit of the FEC engine.

Block interleaving simply consists of a single (*d* x *n*) matrix permutation. The matrix consists of *d* rows (the *interleaver depth*) of the *n*-symbol wide codewords (blocks) generated by the RS encoding process. Hence, the matrix consists of *n* columns. The sole purpose of the *Multiple Codeword Buffer* in Figure 3.1.3.3 is to accumulate codewords (blocks) and provide the block interleaver with a matrix of codewords (blocks). Let the following table represent a codeword (block) matrix:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 8 | 9 | 10 | 11 | 12 | 13 | 14 |
| 15 | 16 | 17 | 18 | 19 | 20 | 21 |
| 22 | 23 | 24 | 25 | 26 | 27 | 28 |
| 29 | 30 | 31 | 32 | 33 | 34 | 35 |

**Table 1.** Depicting a block matrix with five blocks (codewords). Each block comprises a single row and are colored differently to illustrate this point. There are seven columns to illustrate the point that we are dealing with seven-symbol wide blocks (codewords). The *interleaver depth* of this block interleaver is obviously 5 because there are five rows.

Each block is written into the block matrix *row-by-row* (e.g. from the top to bottom). The magic of block interleaving consists of the fact that the matrix is transmitted by reading the matrix *column-by-column* (e.g. from the left to right). For instance, the matrix of Table 1 may be filled as follows:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 |

The matrix will be *block interleaved* into the following sequence and transmitted further down the FEC encoding chain:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1 | 8 | 15 | 22 | 29 | 2 | 9 | 16 | 23 | 30 | 3 | 10 | 17 | 24 | 31 | 4 | 11 | 18 | 25 | 32 | 5 | 12 | 19 | 26 | 33 | 6 | 13 | 20 | 27 | 34 | 7 | 14 | 21 | 28 | 35 |

Let us now demonstrate the power of block interleaving in augmenting the Reed-Solomon error-correcting capabilities. Let us assume that (7, 3) RS code generated the codewords in the matrix of Table 1. We know that the (7, 3) RS code can correct up to two symbol errors in a given codeword. Let us imagine that we elected to not use a block interleaver at all and just transmit the first of first of two matrices shown above. By a stroke of pure bad luck, let us assume that the *entire* third codeword gets corrupted by bursty noise. The result is shown in the following matrix (the red values represent burst error):

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | **15** | **16** | **17** | **18** | **19** | **20** | **21** | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 |

We see that there are seven symbol errors within a codeword and the (7, 3) RS code cannot correct for this many symbol errors. Let us block interleave the symbol stream this time around:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1 | 8 | 15 | 22 | 29 | 2 | 9 | 16 | 23 | 30 | 3 | 10 | 17 | 24 | **31** | **4** | **11** | **18** | **25** | **32** | **5** | 12 | 19 | 26 | 33 | 6 | 13 | 20 | 27 | 34 | 7 | 14 | 21 | 28 | 35 |

Let us now de-interleave the symbol stream:

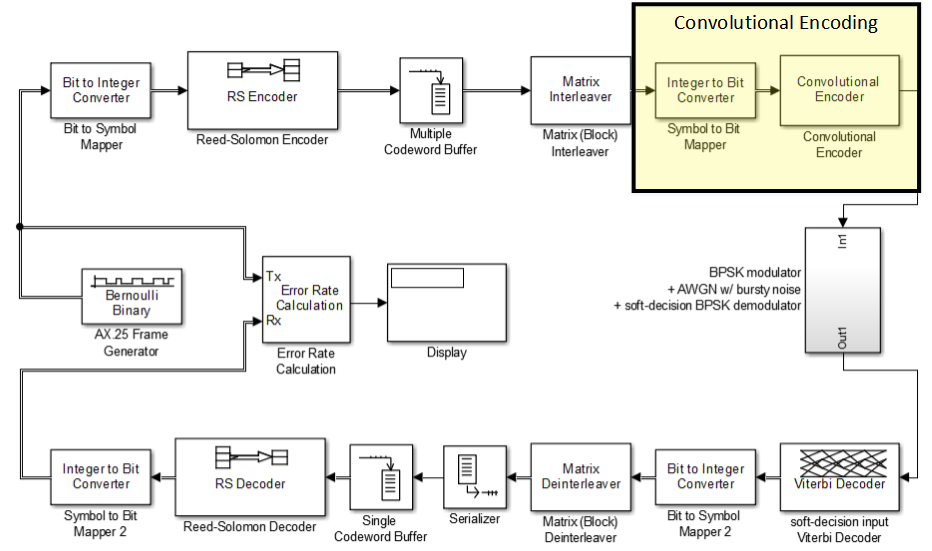
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1 | 2 | 3 | **4** | **5** | 6 | 7 | 8 | 9 | 10 | **11** | 12 | 13 | 14 | 15 | 16 | 17 | **18** | 19 | 20 | 21 | 22 | 23 | **24** | **25** | 26 | 27 | 28 | 29 | 30 | **31** | **32** | 33 | 34 | 35 |

We can see now that no single codeword consists of more than two symbol errors. Hence, the (7, 3) RS code would succeed in correcting for the entire burst error. One can easily imagine how increasing the interleaver depth can spread burst errors apart even further. In general, if a propagation channel causes *b* symbol errors in contiguous fashion, then the interleaver depth (*d*) is calculated as follows:

where *t* is the maximum number of symbol errors within a single codeword that a given RS code can correct.

However, the disadvantage of increasing the interleaving depth is that besides from using slightly more hardware resources, the time required by *Multiple Codeword Buffer* for filling the block matrix increases as well. The higher the interleaving depth, the higher the delay in the digital communication system. This senior design team must be cognizant of this during the design of System C.

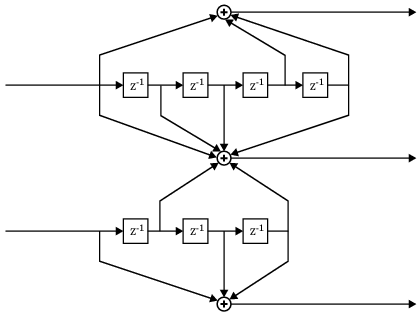
**Convolutional Encoding (and Decoding)**

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**Figure 3.1.3.4** Highlights the convolutional encoder of the FEC engine.

To finish off the coding chain of the forward error correction (FEC) engine, we pass the block-interleaved output through a convolutional encoding process. As discussed in Section 1.3.1, convolutional encoding corrects random errors in a bit stream much better than block encoding does. Unlike block encoding, convolutional encoding operates on a *stream* of bits (as opposed to *blocks* of bits). Further, this implies that the convolutional encoding process operates on a bit stream, not a symbol stream. In Figure 3.1.3.4, there is an *Integer to Bit Mapper* used to convert the symbols of the block-interleaved output back to bits before passing through the convolutional encoder.

The convolutional encoder works by converting a series of *k*-bit message word into a series of *n*-bit codewords. A constraint length *K* represents how many *k-bit* message words are used to process the *n-bit* output of the convolutional encoder. This would be regarded as a (*n*, *k*, *K*) convolutional encoder. The convolutional encoder is composed of a shift register with *K* *k-bit* stages and *n* modulo-2 adders. As an example, Figure 3.1.3.5 shows an example of two convolutional encoders operating in parallel. The upper convolutional encoder comprises *K = 5* stages (or, *K – 1* = 4 *k*-bit delays) in its shift register and *n* = 2 modulo-2 adders. Each stage of the shift register holds *k* = 1 bits. Put differently the upper convolutional encoder is (2, 1, 5). The lower convolutional encoder comprises *K* = 4 stages (or, *K –* 1 = 3 *k*-bit delays) and *n = 2* modulo-2 adders. Each stage of this shift register holds *k* = 1 bits. Hence, the lower convolutional encoder is (2, 1, 4). The *code rate* of a convolutional encoder is *k/n*, so the code rates for the upper and lower convolutional encoders would be ½, respectively.



**Figure 3.1.3.5** (Courtesy of Matlab®) Depicting two convolutional encoders operating in parallel.

At each unit of time, *k* bits will shift to the next stage in the shift register, and *k* bits will shift into the first stage of the shift register. There are *K* stages for a group of *k* bits to shift into before it eventually shifts out of the shift register. At each unit of time, each of the *n* modulo-2 adders are sampled and these *n* bits are the output of the convolutional encoder. The connections between the shift register stages and the modulo-2 adders characterizes the convolutional encoder. In other words, some permutations of connections have better error-correcting capabilities than other permutations of connections (Sklar, 2001).

The soft-decision Viterbi decoder uses Euclidean distance and maximum likelihood to decode the convolutional encoding.

## Hardware Implementation using ISE Design Suite

# EVALUATION (Brandon)

Deep space and satellite communication links are riddled with random errors across a very wide bandwidth (Nguyen, et. al, 2009). In addition to random errors in the satellite link, bursts of noise can corrupt an entire segment of a link resulting in burst errors (Murphy, et. al, 1994). These channel imperfections are common in satellite communications and are modeled very well by the additive white Gaussian noise (AWGN) channel (Viswanathan, 2013). The AWGN channel is a random noise channel that makes a communication link vulnerable to random bit errors and burst errors. In general, it is understood that AWGN provides maximum bit corruption and compared to other channel models, systems that perform the best in AWGN perform the best in real-life situations (Viswanathan, 2013). Hence, this senior design project will rely solely on the AWGN channel (see Section 1.3.6) to represent the propagation medium for our three amateur radio satellite telemetry systems.

We implement the bit error rate tester (BERT) in software. The BERT consists of an AX.25 packet generation program written by us, a custom AX.25 packet comparison program written by us, and an available virtual serial terminal interface (with data logging capabilities). The BERT provides several performance metrics based off of bit error rate (BER) and packet error rate (PER). Please refer to Section 3 (Approach) for the implementation of this BERT and how it interfaces with the external FPGA board.

# SUMMARY AND FUTURE WORK

# ACKNOWLEDGEMENTS

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1. Product SPECIFICATION
2. SOME INTERESTING RELEVANT DERIVATION